REAL-TIME LOAD BALANCING AND POWER FACTOR CORRECTION OF THREE-PHASE, FOUR-WIRE UNBALANCED SYSTEMS WITH DSTATCOM

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ABSTRACT

This paper presents the design and implementation of a distribution-level static synchronous compensator (DSTATCOM) used for the real-time load compensation of three-phase, four-wire power distribution systems with unbalanced loads. First, use of the symmetrical components method derives a feed-forward compensation scheme for the DSTATCOM. The system block diagram of the DSTATCOM is then built. A computer simulation is performed for preliminary verification. Finally, a hardware prototype is built using a TMS320C6711-based controller. Experimental results verify the functionality of the DSTATCOM.

I. INTRODUCTION

An unbalanced inductive load in a three-phase, four-wire electric power distribution system produces undesired negative- and zero-sequence currents with a lagging power factor, which causes additional system losses in the power distribution system and an unbalanced voltage drop on the distribution line. The unbalanced voltage drop results in an unbalanced voltage on the load bus, affecting other sensitive loads connected at the bus. The negative- and zero-sequence currents are considered poor power quality phenomena and should be avoided when the unbalanced load bus voltage jeopardizes the sensitive loads connected to the system [8].

Load compensation signifies balancing an unbalanced load and correcting the load power factor to unity simultaneously.

Load compensation is critical for electric power distribution system that feeds a large capacity of unbalanced loads with lagging power factors, such as those in a single-phase electrical railway and electric arc furnace systems.

Since 1970, static var compensators (SVCs) have been widely used in the electric power industry to enhance power system performances in areas such as voltage regulation, voltage flicker mitigation, power factor correction, and unbalanced load balancing [7, 9, 11, 12]. Recently, because of rapid development of high-power switching elements such as insulated gate bipolar transistors (IGBTs) and integrated gate commutated thyristors (IGCTs), static synchronous compensators (STATCOMs) have been recognized as the next generation of compensators [1, 3, 6, 10, 15-17]. The distribution-level static synchronous compensator (DSTATCOM) is a newly developed STATCOM used in electric power distribution systems. Compared to existing SVCs, DSTATCOMs require less space and are quicker, more compact, and quieter. In addition, recent research has shown that DSTATCOMs greatly enhance the low-voltage ride-through (LVRT) abilities of wind farms [4, 13, 14].

This paper proposes a DSTATCOM for the real-time load compensation of three-phase, four-wire power distribution systems with unbalanced inductive loads. A new feedforward compensation scheme is derived enabling the DSTATCOM to quickly balance the unbalanced load and correct the load power factor to unity simultaneously. A three-phase, four-wire unbalanced system incorporating the proposed DSTATCOM is built and simulated with the MATLAB/Simulink software package. A hardware prototype is then built for testing. Finally, experimental results are given for verification.

II. DSTATCOM COMPENSATION SCHEME

1. Derivation of the Compensation Scheme

Fig. 1 shows a three-phase, four-wire power distribution system feeding an unbalanced load. A DSTATCOM is installed in parallel with the unbalanced inductive load. In the paper, the DSTATCOM is equivalent to a current-controlled
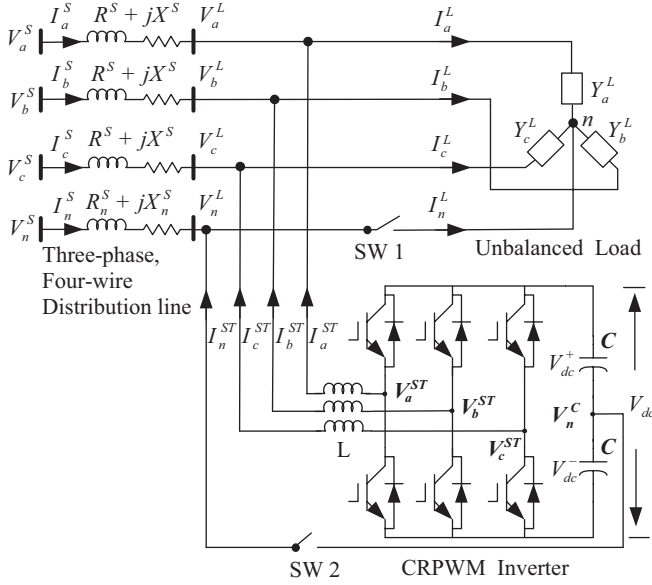
Fig. 1. A three-phase, four-wire electric power distribution system with an unbalanced load and a DSTATCOM.

source. To compensate an unbalanced load, a feedforward compensation scheme is used for the DSTATCOM. The DSTATCOM controller detects the load power data, calculates the required compensation current output according to the load compensation scheme, and generates a current in each phase to compensate the negative- and zero-sequence currents caused by the unbalanced load. By using the DSTATCOM compensation, the power source provides only balanced active power.

The symmetrical components method is used to derive the feedforward compensation scheme of the proposed DSTATCOM. As shown in Fig. 1, the line-to-neutral load voltages are transferred to positive-, negative-, and zero-sequence components by using the symmetrical components transformation matrix $[T]$, expressed in Eq. (1).

$$\begin{bmatrix} \bar{V}_a^L \\ \bar{V}_b^L \\ \bar{V}_c^L \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & \alpha^2 & \alpha \\ 1 & \alpha & \alpha^2 \end{bmatrix} \begin{bmatrix} \bar{V}_0^L \\ \bar{V}_1^L \\ \bar{V}_2^L \end{bmatrix} = [T] \begin{bmatrix} \bar{V}_0^L \\ \bar{V}_1^L \\ \bar{V}_2^L \end{bmatrix}, \; \alpha = e^{j(2/3)\pi} \quad (1)$$

The line-to-neutral voltages are assumed to be balanced to simplify the derivation of the compensation scheme, as expressed in Eq. (2). The three-phase load currents in the *a-b-c* reference frame can be expressed as Eqs. (3)-(5). Applying the symmetrical components method transfers the three-phase load currents to the positive-, negative-, and zero-sequence components, as expressed in Eqs. (6)-(8).

$$\bar{V}_a^L = \bar{V}_p^L = V_p^L \angle 0^\circ, \; \bar{V}_b^L = \alpha^2 \bar{V}_p^L, \; \bar{V}_c^L = \alpha \bar{V}_p^L \quad (2)$$

$$\bar{I}_a^L = Y_a^L \bar{V}_p^L \quad (3)$$

$$\bar{I}_b^L = \alpha^2 Y_b^L \bar{V}_p^L \quad (4)$$

$$\bar{I}_c^L = \alpha Y_c^L \bar{V}_p^L \quad (5)$$

$$\bar{I}_0^L = \frac{1}{3}[Y_a^L + \alpha^2 Y_b^L + \alpha Y_c^L]V_p^L \quad (6)$$

$$\bar{I}_1^L = \frac{1}{3}[Y_a^L + Y_b^L + Y_c^L]V_p^L \quad (7)$$

$$\bar{I}_2^L = \frac{1}{3}[Y_a^L + \alpha Y_b^L + \alpha^2 Y_c^L]V_p^L \quad (8)$$

To achieve real-time load compensation, the DSTATCOM should compensate for the imaginary part of the positive-sequence load current and the entire negative- and zero-sequence load currents, as expressed in Eq. (9). Thus, the power source supplies only the real part of the positive-sequence load current. The required compensation current for the DSTATCOM can be expressed as Eqs. (10)-(12).

$$\bar{I}_0^C = \bar{I}_0^L, \; \bar{I}_1^C = \text{Im}[\bar{I}_1^L], \; \bar{I}_2^C = \bar{I}_2^L \quad (9)$$

$$\bar{I}_a^C = \text{Im}[\bar{I}_1^L] + \bar{I}_2^L + \bar{I}_0^L \quad (10)$$

$$\bar{I}_b^C = \alpha^2 \text{Im}[\bar{I}_1^L] + \alpha \bar{I}_2^L + \bar{I}_0^L \quad (11)$$

$$\bar{I}_c^C = \alpha \text{Im}[\bar{I}_1^L] + \alpha^2 \bar{I}_2^L + \bar{I}_0^L \quad (12)$$

The load power of the three-phase, four-wire system can be determined using the three-wattmeter method, expressed in Eqs. (13)-(15), rearranging Eqs. (13)-(15) yields Eq. (16), in which the positive-, negative-, and zero-sequence load currents are represented with line-to-neutral active and reactive powers.

$$(\bar{V}_a^L)^* (\bar{I}_a^L) = V_p^L[\bar{I}_1^L + \bar{I}_2^L + \bar{I}_0^L] \quad (13)$$

$$(\bar{V}_b^L)^* (\bar{I}_c^L) = \alpha^2 \cdot V_p^L[\alpha^2 (\bar{I}_1^L) + \alpha(\bar{I}_2^L) + (\bar{I}_0^L)] \quad (14)$$

$$(\bar{V}_c^L)^* (\bar{I}_c^L) = \alpha \cdot V_p^L[\alpha(\bar{I}_1^L) + \alpha^2(\bar{I}_2^L) + (\bar{I}_0^L)] \quad (15)$$

$$\begin{bmatrix} \bar{I}_1^L \\ \bar{I}_2^L \\ \bar{I}_0^L \end{bmatrix} = \frac{1}{3V_p^L} \begin{bmatrix} 1 & 1 & 1 \\ 1 & \alpha & \alpha^2 \\ 1 & \alpha^2 & \alpha \end{bmatrix} \begin{bmatrix} P_a^L - jQ_a^L \\ P_b^L - jQ_b^L \\ P_c^L - jQ_c^L \end{bmatrix} \quad (16)$$

Finally, combining Eqs. (10)-(12) and (16) obtains the currents required by the DSTATCOM for real-time unbalanced load compensation, expressed in Eq. (17).
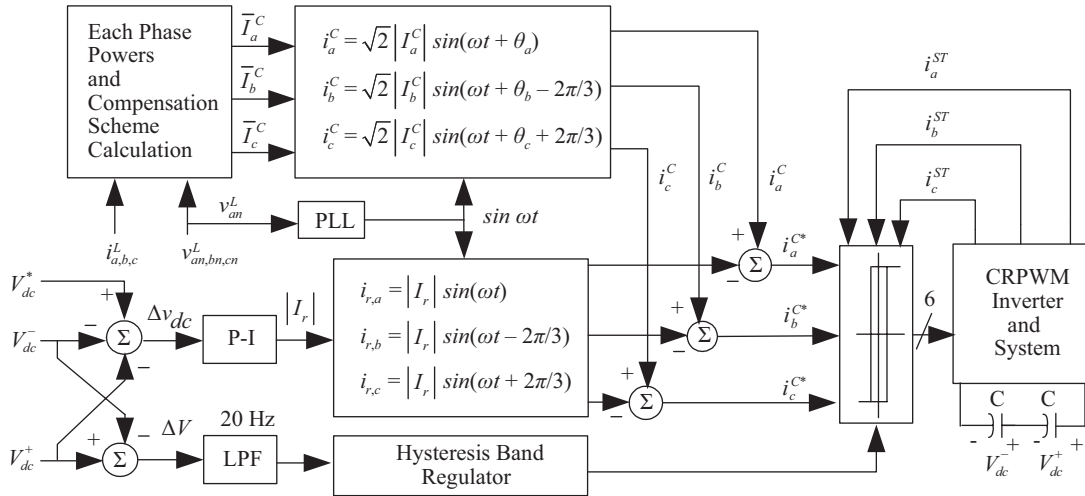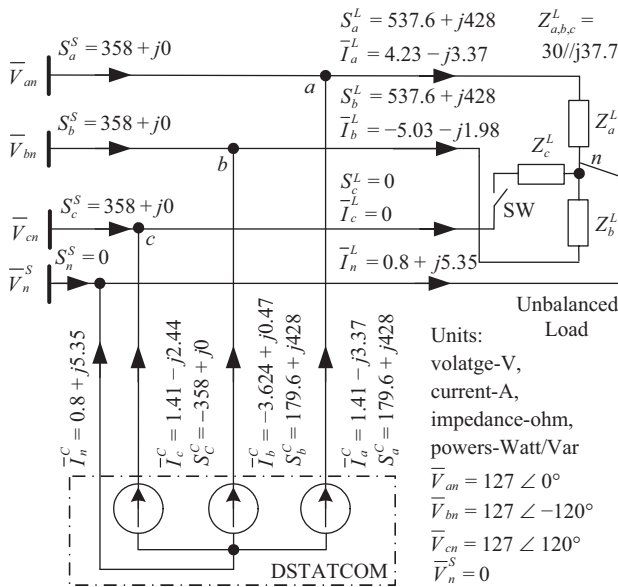
Fig. 3. Block diagram of the DSTATCOM controller.

Fig. 2. An illustrating example for three-phase, four-wire unbalanced load compensation.

$$\begin{bmatrix} \overline{I}_a^C \\ \overline{I}_b^C \\ \overline{I}_c^C \end{bmatrix} = [H] \begin{bmatrix} P_a^L/V_p^L \\ Q_a^L/V_p^L \\ P_b^L/V_p^L \\ Q_b^L/V_p^L \\ P_c^L/V_p^L \\ Q_c^L/V_p^L \end{bmatrix} \qquad (17)$$

where the matrix $[H]$ is:

$$\begin{bmatrix} 2/3 & 1\angle-90° & -1/3 & 0 & -1/3 & 0 \\ 1\angle60°/3 & 0 & 2\angle-120°/3 & 1\angle150° & 1\angle60°/3 & 0 \\ 1\angle-60°/3 & 0 & 1\angle-60°/3 & 0 & 2\angle120°/3 & 1\angle30° \end{bmatrix}$$

2. Illustrative Example

Fig. 2 shows an example of the three-phase, four-wire unbalanced load compensation using the proposed DSTATCOM. Phase-*c* of the load is opened to create an unbalanced operation absorbing unbalanced line currents with lagging power factors. The DSTATCOM uses Eq. (17) as the compensation scheme for unbalanced load compensation. In addition, Fig. 2 lists calculated power flow data, including line currents and the powers of the source, load, and DSTATCOM. By using the DSTATCOM compensation, the power source only provides balanced active power. The calculation results in Fig. 2 indicate that even though the DSTATCOM does not produce active power, it provides a path for redistributing the load power flow for load compensation.

3. DSTATCOM Controller Block Diagram

Fig. 3 shows the block diagram of the proposed DSTATCOM controller. The real-time load data, $P_{a,b,c}^L$, $Q_{a,b,c}^L$, and V^L, are obtained using the fast power data detection method described in [2]. The DSTATCOM is equivalent to a current-controlled source in this paper. Eq. (17) is used to calculate the compensation currents. Using a phase-locked loop (PLL) generates the reference angle of the load bus voltage. The instantaneous compensation current command $i_{a,b,c}^C$ for the load compensation is obtained. A current-regulated pulse-width modulated (CRPWM) inverter is employed as the power stage of the DSTATCOM to generate the compensation current. To maintain the dc-link voltage of the DSTATCOM inverter at an assigned level, supply the power losses, and charge the dc-link capacitors, the DSTATCOM must absorb active power from the power source. A P-I type feedback controller regulates the real-part current $|I_r|$ of the DSTATCOM, as expressed in Eq. (18). The active current $|I_r|$ is then transferred as part of the compensation current commands, expressed in Eq. (19). The signal *sin ωt* from the PLL generates the real part of the

instantaneous compensation currents $i_{r,(a,b,c)}$.

$$\left|I_r\right| = K_p \Delta v_{dc} + K_i \int \Delta v_{dc} dt, \ \Delta v_{dc} = V_{dc}^* - V_{dc} \qquad (18)$$

$$\begin{bmatrix} \overline{I}_{r,a} \\ \overline{I}_{r,b} \\ \overline{I}_{r,c} \end{bmatrix} = \begin{bmatrix} 1\angle 0 \\ 1\angle -2\pi/3 \\ 1\angle 2\pi/3 \end{bmatrix} \left|I_r\right| \qquad (19)$$

Combining the compensation current demands $i_{a,b,c}^C$ for the load compensation and the real-part currents in Eq. (19) for the dc-link voltage support yields the required compensation current command, as expressed in Eq. (20).

$$i_{a,b,c}^{C*} = i_{a,b,c}^C - i_{r,(a,b,c)} \qquad (20)$$

As shown in Fig. 1, a voltage deviation $\Delta V = (V_{dc}^+ - V_{dc}^-)$ is generated on the two dc-link capacitors connected serially because of the control error and the interference of zero-sequence current. A hysteresis bandwidth control should be used for balancing [5], as shown in Fig. 3. Using a low-pass filter with a bandwidth of 20 Hz removes the 60 Hz fundamental signal in the dc-link voltage deviation signal ΔV. A hysteresis band regulator receives the output signal and controls the hysteresis band of the hysteresis current comparator. Combining the current command signals i_a^{C*}, i_b^{C*}, i_c^{C*} and actual DSTATCOM output currents i_a^{ST}, i_b^{ST}, i_c^{ST} determines the error currents. The CRPWM control signals are obtained using the hysteresis current comparator and are used to control the switching elements in the DSTATCOM main circuit. Thus, the actual compensation current can track the command signal, and DSTATCOM operation is achieved.

III. SIMULATION RESULTS

The MATLAB/Simulink software package is used to preliminarily verify the functionality of DSTATCOM. Figs. 1 and 3 are used to construct the simulation system. The system parameters are $V_{ll}^S = 220$ V, $L = 15$ mH, $Z^s = 0.1 + j1$ Ω, $C = 2,200$ μF, and $f_s = 60$ Hz. A phase-opened operation is established using phase-c as a disturbance. In addition to three-phase, four-wire system compensation, the proposed DSTATCOM is effective in a three-phase, three-wire system, thus, simulations are conducted for both systems.

1. Three-Phase, Four-Wire System Compensation

Fig. 4 shows the simulation results for three-phase, four-wire unbalanced load compensation. The initial operation point is set at a balanced operation with $P_{3\phi}^L = 4.8$ kW, $Q_{3\phi}^L = 3.6$ kVar, and pf = 0.8 lagging. At $t = 0.01$ s, phase-c of the load is suddenly opened to create an unbalanced load operation, as

(a) Three-phase load currents $i_{a,b,c}^L$

(b) Three-phase compensation currents $i_{a,b,c}^{ST}$

(c) Three-phase source currents $i_{a,b,c}^S$

(d) Powers from the source

(e) Powers to the load

(f) Neutral current in the source and load

(g) Dc-link voltages response
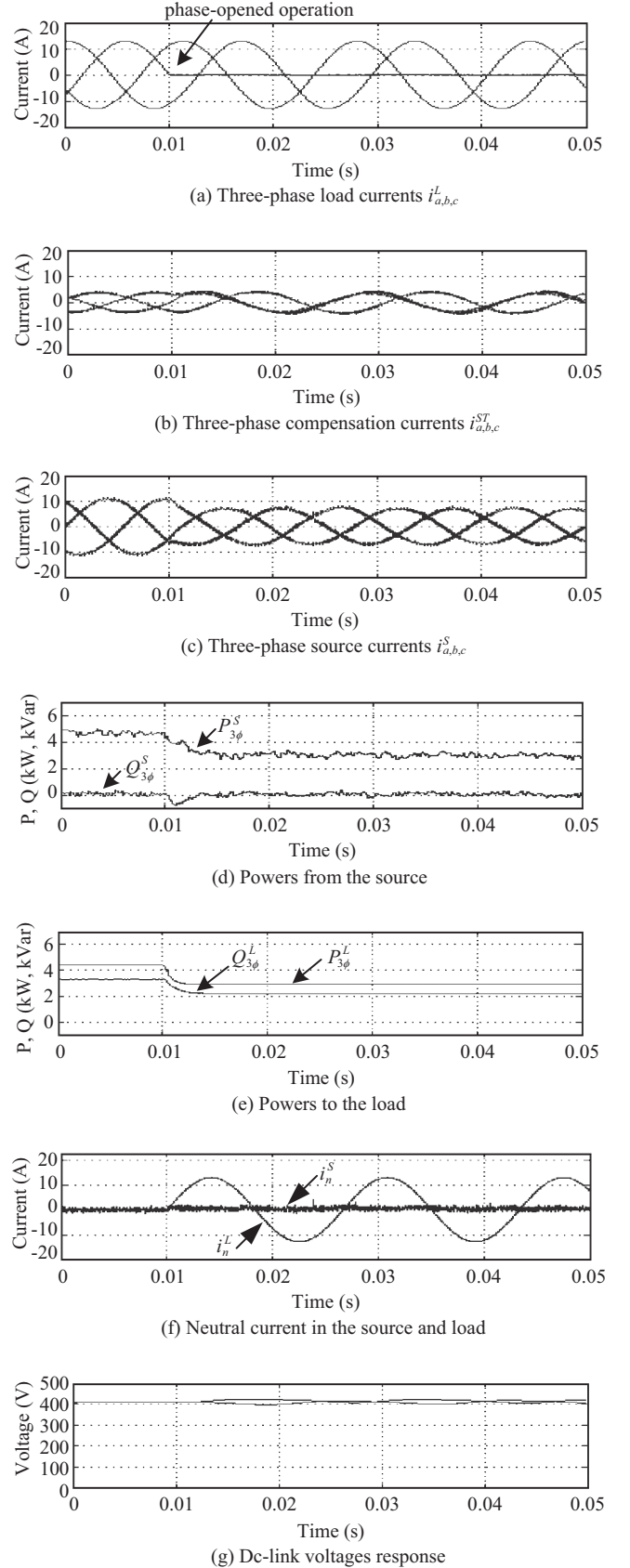
Fig. 4. **Transient response for an opened-phase operation with the DSTATCOM compensation.**

(a) Three-phase load currents $i_{a,b,c}^{L}$

(b) Three-phase source currents $i_{a,b,c}^{S}$

(c) Three-phase compensation currents $i_{a,b,c}^{ST}$

(d) Powers from the source

(e) Powers to the load

(f) Positive-sequence component currents

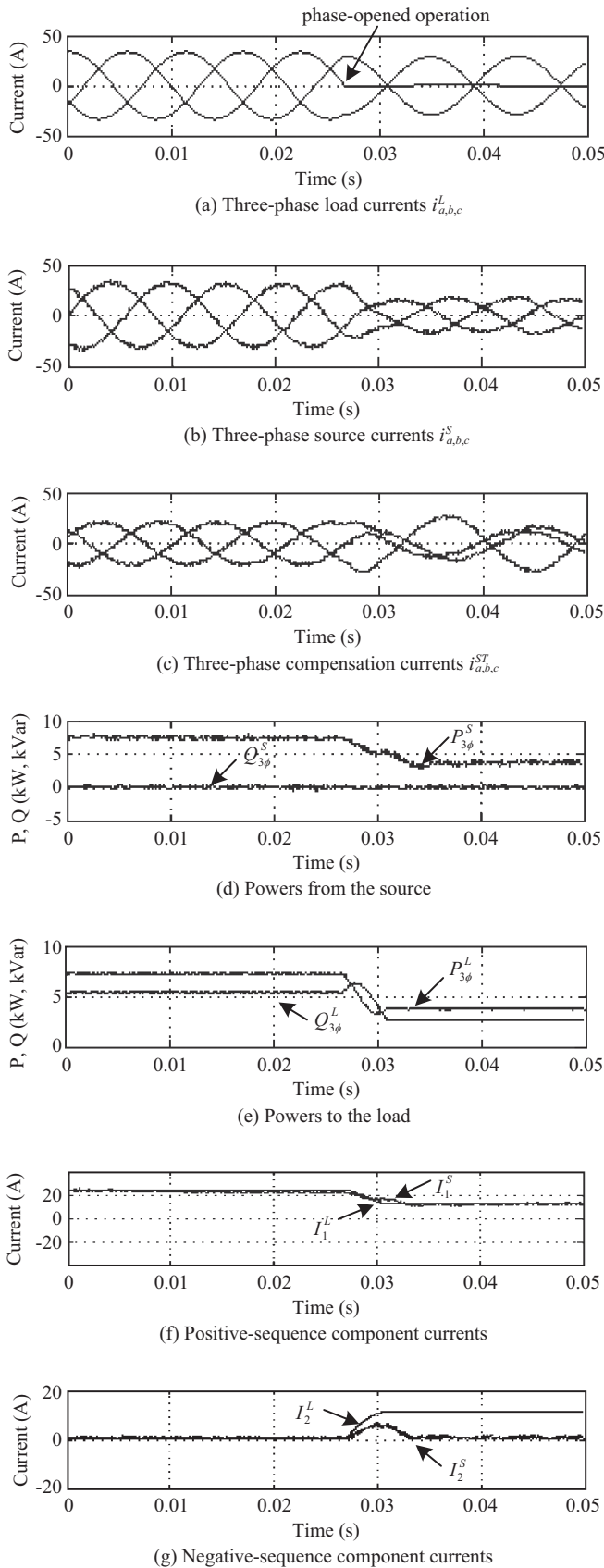(g) Negative-sequence component currents

Fig. 5. Transient compensation response with the DSTATCOM compensation.

shown in Fig. 4(a). Phase-*c* load current is reduced to zero. As shown in Fig. 4(b), the DSTATCOM regulates the compensation currents to unbalanced operation in accordance with the load compensation scheme. Because of the DSTATCOM compensation, the three-phase source currents remain in a balanced and unity power factor condition, as shown in Figs. 4(c) and (d). Although the unbalanced load generates a neutral current, as shown in Fig. 4(f), the neutral current from the source is eliminated quickly by the DSTATCOM compensation. Fig. 4(g) shows that the voltages on the two dc-link capacitors constantly remain in balanced operation. The proposed DSTATCOM for the three-phase, four-wire unbalanced load compensation is rapid and effective.

2. Three-Phase, Three-Wire System Compensation

Fig. 5 shows the compensation results of the DSTATCOM for three-phase, three-wire unbalanced load compensation. In the simulation, the switches SW1 and SW2 (Fig. 1) are opened for three-phase, three-wire system operation. The system is initially operated with $P_{3\phi}^{L} = 7.2$ kW, $Q_{3\phi}^{L} = 5.4$ kVar, and pf = 0.8 lagging. At $t = 0.027$ s, the phase-*a* of the load is opened, as shown in Fig. 5(a). Because of the DSTATCOM compensation, the source currents are balanced and corrected to unity power factor, as shown in Figs. 5(b) and (d). Figs. 5(f) and (g) show the transient responses of the positive and negative components, respectively, of the source and load currents. The DSTATCOM response time is approximately 4 ms. The simulation results preliminarily verify that the proposed DSTATCOM is appropriate for the real-time load compensation of both three-phase, three-wire and three-phase, four-wire systems with unbalanced inductive loads.

IV. HARDWARE SYSTEM SETUP AND EXPERIMENTAL VERIFICATION

Fig. 6 shows the block diagram of the implemented hardware prototype system. A three-phase, four-wire distribution system is constructed for a verification test. Table 1 lists the system parameters, which are the same as those shown in Fig. 2. A digital signal processor (DSP) TMS320C6711 - based control system is employed as the DSTATCOM controller. The control program is edited in a host PC using C language. The execution file is then downloaded onto the DSP-based controller for real-time control of the DSTATCOM. During the DSTATCOM compensation, the three-phase source currents, load currents, and load bus voltages are obtained by the DSP and uploaded to the host PC for analysis. Because of the floating-point handling ability of the DSP, the DSTATCOM is capable of real-time load compensation.

Fig. 7 shows the DSTATCOM compensation test results. In the test, a phase-opened operation is set as a disturbance. The system begins in a balanced condition. At $t = 0.062$ s, a phase-opened operation is activated in phase-*c*, which creates an unbalanced load operation, and the functionality of the DSTATCOM is tested. Figs. 7(a) to (c) show the three-phase
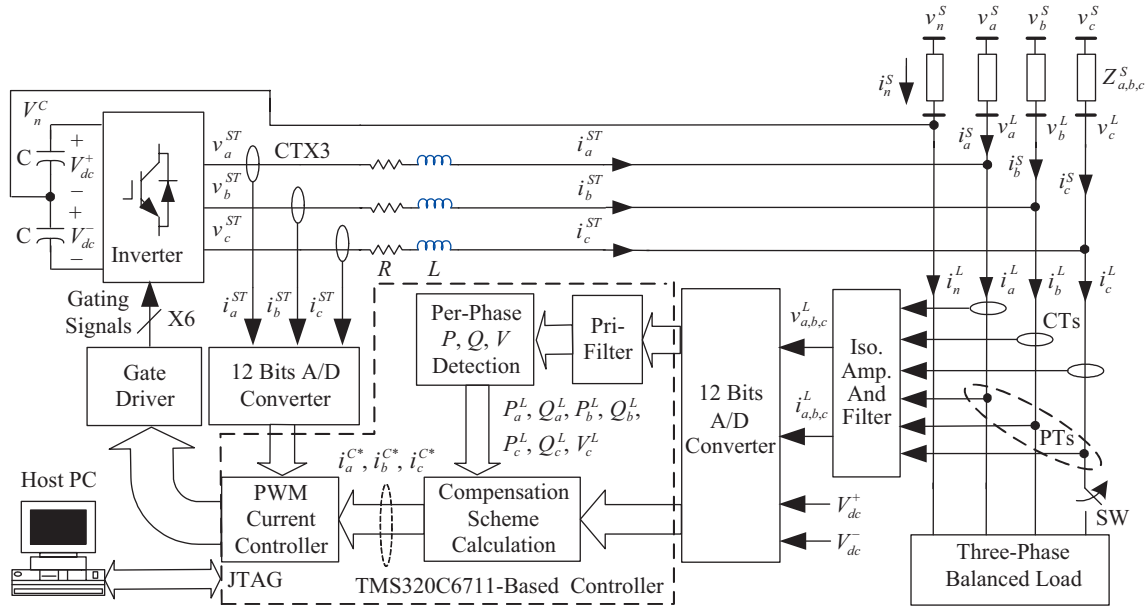
Fig. 6. Block diagram of the DSTATCOM hardware system setup.

Table 1. The hardware system parameters.

Power source	$V_{ll}^S = 220\,V$, $f_s = 60\,Hz$, $Z^S = 0.1 + j1\,\Omega$
DSTATCOM	$L = 15\,mH$, $R = 0.5\,\Omega$, $C = 2,200\,\mu F$
	$V_{dc} = 400\,V$, $f_{PWM} = 5\,kHz$
Load	$R^L = 30\,\Omega // X^L = 37.7\,\Omega$, Y-connection

load currents, the compensation currents, and the source currents responses, respectively. At $t = 0.062$ s, the phase-c load current suddenly decreases to zero, as shown in Fig. 7(a). After the phase-opened operation, the DSTATCOM three-phase compensation currents become unbalanced, as shown in Fig. 7(b). The three-phase source currents are then balanced, as shown in Fig. 7(c). Fig. 7(d) shows that the phase-a source current constantly remains in phase with the phase-a voltage, verifying unity power factor correction.

Fig. 8 shows the power levels and neutral current responses with the DSTATCOM compensation. Figs. 8(a) and (b) show the power levels from the source and to the load. Although the load requires reactive power during operation, the source supplies only active power. The reactive power from the source is constantly reduced to zero by the DSTATCOM. Fig. 8(c) shows the neutral currents of the source and load. Because of the DSTATCOM compensation, the neutral current from the source is eliminated quickly. The experimental results reveal that the proposed DSTATCOM is highly appropriate for the real-time load compensation of a three-phase, four-wire power system.

V. CONCLUSIONS

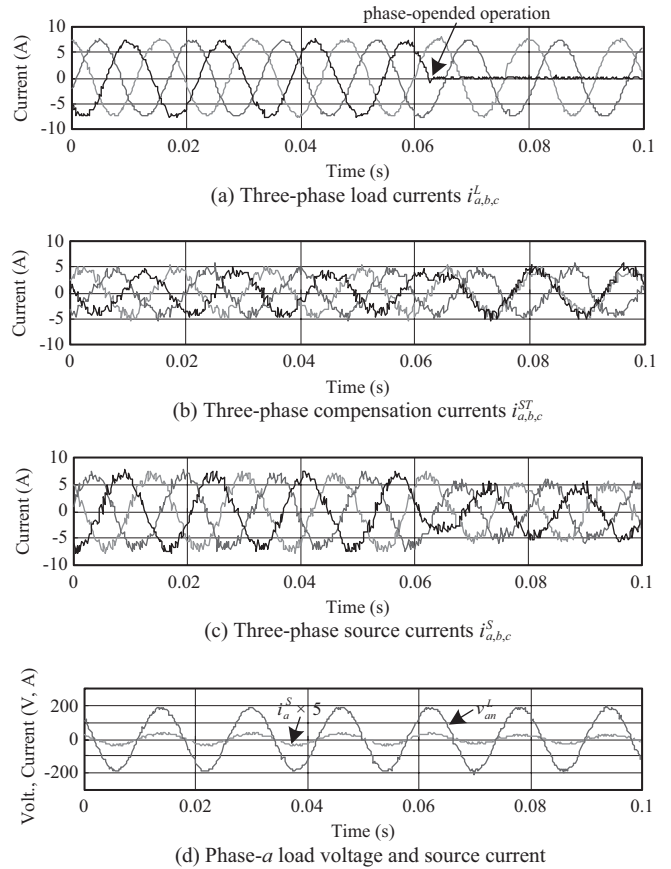This paper presents the design and implementation of a DSTATCOM for fast load compensation in a three-phase,

(a) Three-phase load currents $i_{a,b,c}^L$

(b) Three-phase compensation currents $i_{a,b,c}^{ST}$

(c) Three-phase source currents $i_{a,b,c}^S$

(d) Phase-a load voltage and source current

Fig. 7. System responses for an opened-phase operation with the DSTATCOM compensation.

four-wire power distribution system with an unbalanced inductive load. To satisfy the rapid response requirement, a new

(a) Powers to the load

(b) Powers from the source
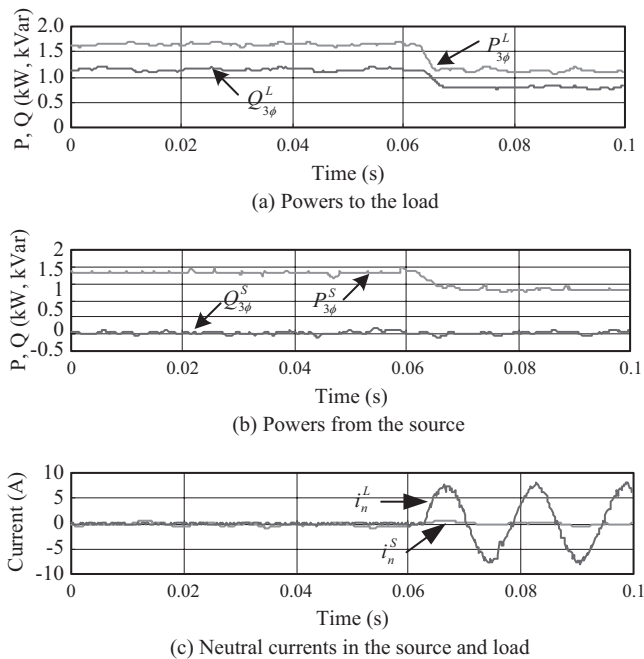

(c) Neutral currents in the source and load

Fig. 8. Powers and neutral currents responses with the DSTATCOM compensation.

feedforward compensation scheme is employed using the symmetrical components method, therefore, the modeling and control of the DSTATCOM is similar to that of traditional SVCs. Simulation results from the MATLAB/Simulink software package show that the proposed DSTATCOM has a rapid response time and exerts an accurate compensation effect. A hardware prototype employing a TMS320C6711 floating-point DSP-based system is built for the final verification test. Experimental results show that the proposed DSTATCOM is highly effective for rapid load compensation. DSTATCOMs may gradually replace static var compensators in the near future.

LIST OF SYMBOLS

<u>General</u>

Re	= real part
Im	= imaginary part
S	= complex power
P	= active power
Q	= reactive power
V	= voltage
I	= current
Z	= impedance
Y	= admittance
X	= reactance
R	= resistance

<u>Subscripts</u>

a,b,c	= phase-a, -b, -c
n	= neutral
p	= phase
0	= zero-sequence component
1	= positive-sequence component
2	= negative-sequence component
dc	= direct current
r	= active (real) part
3ϕ	= three-phase
ll	= line-to-line

<u>Superscripts</u>

S	= source
L	= load
C	= compensation
ST	= DSTATCOM
$*$	= complex conjugate or command

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