



A Reversible Three-Phase Step Up/Down Switching Mode Rectifier

Jenn-Jong Shieh

Associate Professor, Department of Electrical Engineering, Ta Hwa Institute of Technology, Chiunglin, Hsinchu Hsien, Taiwan 30740, R.O.C., eesjj@et4.thit.edu.tw

Follow this and additional works at: <https://jmstt.ntou.edu.tw/journal>



Part of the [Electrical and Computer Engineering Commons](#)

Recommended Citation

Shieh, Jenn-Jong (2002) "A Reversible Three-Phase Step Up/Down Switching Mode Rectifier," *Journal of Marine Science and Technology*. Vol. 10: Iss. 2, Article 7.

DOI: 10.51400/2709-6998.2310

Available at: <https://jmstt.ntou.edu.tw/journal/vol10/iss2/7>

This Research Article is brought to you for free and open access by Journal of Marine Science and Technology. It has been accepted for inclusion in Journal of Marine Science and Technology by an authorized editor of Journal of Marine Science and Technology.

A Reversible Three-Phase Step Up/Down Switching Mode Rectifier

Acknowledgements

The author gratefully thanks the financial support of the National Science Council of Taiwan, R.O.C. through grant number NSC 90-2213-E-233-003.

A REVERSIBLE THREE-PHASE STEP UP/DOWN SWITCHING MODE RECTIFIER

Jenn-Jong Shieh*

Key words: null space vector, switching mode rectifier, model.

ABSTRACT

In this paper, focus on the null space vector duty cycle control, a reversible three-phase step up/down switching mode rectifier is proposed attain clean sinusoidal input current, unity power factor, bi-directional power flow, step up/down output DC voltage and insensitivity for a voltage input. In addition, a precise simulation model is proposed to simulation by using PC software tools. Finally, some simulation and experimental results are presented for verification.

INTRODUCTION

Recently, the power drive technology for motor drive is very popular in various industrial application such as industrial robots, machine tools etc. In those machine there are traditional utility interface made of diodes or phase-controlled rectifiers. However, the low power factor translates into poor utilization of the available current carrying capacity of the AC distribution system [1,2], then a high harmonic content in the line current frequency creates interference among equipment connected lines. In addition, from the point of view that the harmonic restriction of rectifier factors cannot fit all different kinds harmonic standards such as IEC 1000-3-2 and EN 60555-2 [3-5]. In other words, to obtain a high power quality and satisfy harmonic standards with the utility grid draw as similar as a sinusoidal current is important. So, a lot of research has been made for the area of pulse width modulation(PWM) switching mode rectifiers. On the other hand, for active DC load such as DC or AC motor drives needs the DC voltage with a step up/down DC bus voltage and regeneration capability. To provide the above capabilities, the conventional step-up/down AC/DC conversion may be completed by two cascaded rectifiers. Although this scheme

offers many possibilities, the power delivered to load has been processed twice causing a decrease in the overall efficiency. Some three-phase buck-boost type AC/DC converters in literature have been proposed to offer step-up/down capability [5-10]. However, the disadvantages of pulsating input and/or output currents remain the problem, but unidirectional power flow needs to be overcome. The single-phase SEPIC AC/DC rectifier combines the best features of boost and flyback topologies, making it especially advantageous in high power factor preregulator applications. In addition, the ripple current can be steered away from the input, dramatically reducing input noise filtering requirements [11-13]. In the recently, there are very few papers talk about three-phase SEPIC AC/DC rectifier with bidirectional power flow converter in literature.

In this paper, based on the null space vector duty cycle control, a novel three-phase switching mode interface with its control circuit is proposed to achieve the desired qualities such as clean sinusoidal line current, unity power factor, bidirectional power flow, step up/down output DC voltage and insensitivity to voltage input. Also, the proposed control circuit without the use of multiplier and lock-out circuit implemented in conventional power correction rectifiers. Next an accurate simulation model is presented that can be used for convenient simulation with common PC software tools. In addition, the popularly used state space averaging technique is extended for modeling the proposed rectifier and deriving the voltage transfer ratio. Finally, some simulation and experimental results are processed to verify the validity of the proposed rectifier.

SYSTEM DESCRIPTION OF THE PROPOSED RECTIFIER

A basic block diagram of the proposed switching mode rectifier is shown in Fig. 1. It consists mainly of power stage which switches are MOSFETs and turned on or off independently to active low current distortion, unity power factor, bidirectional power flow and step up/down capability, a feedback controller and a current

Paper Submitted 01/08/02, Accepted 04/12/02. Author for Correspondence: Jenn-Jong Shieh.

**Associate Professor, Department of Electrical Engineering, Ta Hwa Institute of Technology, Chiunglin, Hsinchu Hsien, Taiwan 30740, R.O.C. E-mail: eesjj@et4.thit.edu.tw*

controller. In order to reduce the total harmonic distortion (THD) of the input line current, three filter inductors are used on the AC side. In addition, the DC load is assumed to have resistance R . The control strategy block diagram as shown in Fig. 2 can be easy for understanding the basic operation principle of the proposed rectifier.

There are two control loops in this rectifier. The first one is the current control loop. The sign of the dc voltage error e_v indicates whether the rectifier is operated at rectifier or regeneration mode. In the rectifier (regeneration) mode, a 0 (π) radius phase signal is obtained from the source voltage signal and applied to the reset terminal of the counter. At the same time an oscillator that generates a high frequency clock signal is applied to the clock terminal of the same counter. An output signal from the counter is led to an address terminal of three ROMs that store the sinusoidal data

with $2\pi/3$ phase differences. The sinusoidal waveforms data corresponding to the variation of the signal is obtained from the counter as the address signals is read successively and applied to a data input terminal of three digital-to-analog (D/A) converters. The magnitude of the current command signal I_m^* is obtained from the value of a voltage controller and applied to the reference terminal of the D/A converters to generate the desired reference currents i_k^* , $k = 1, 2, 3$. To force the line current i_k follows the respective reference current signals and obtains unity power factor, bidirectional power flow, step up/down output dc voltage as well as insensitive input voltage, a current controller as shown in Fig. 2 is adopted to generate the desired gating signals of seven switches. It consists of three conventional PWM current controllers and an integrated logic circuit as shown in Fig. 3. For reference, Fig. 4 shows the conceptual gating signals of seven switches for one switching period T_s where the switching frequency is assumed to be much higher than the reference wave m_k , $k = 1, 2, 3$ frequency and $m_1 > m_2 > m_3$. For analysis simplicity, the amplitude of the triangular wave $C(t)$ is normalized, and the magnitude of each reference wave may not exceed one to avoid the presence of low frequency harmonics. As can be observed from Fig. 4, during each switching period there are two portions, namely $d_{n0}T_s$ and $d_{n7}T_s$, where all six active switches of the bridge are closed such that v_{C1} of Fig. 1 can be discharged and supply the inductance L_1 to keep the stage followed the DC SEPIC converter operation principle. As a result, the conduction loss can be minimized. Additionally, to preserve the function of SEPIC converter, switch S_7 should operate complementary for the remaining switching period, namely $[1 - (d_{7a} + d_{7b})]T_s$, where all six switches of the bridge

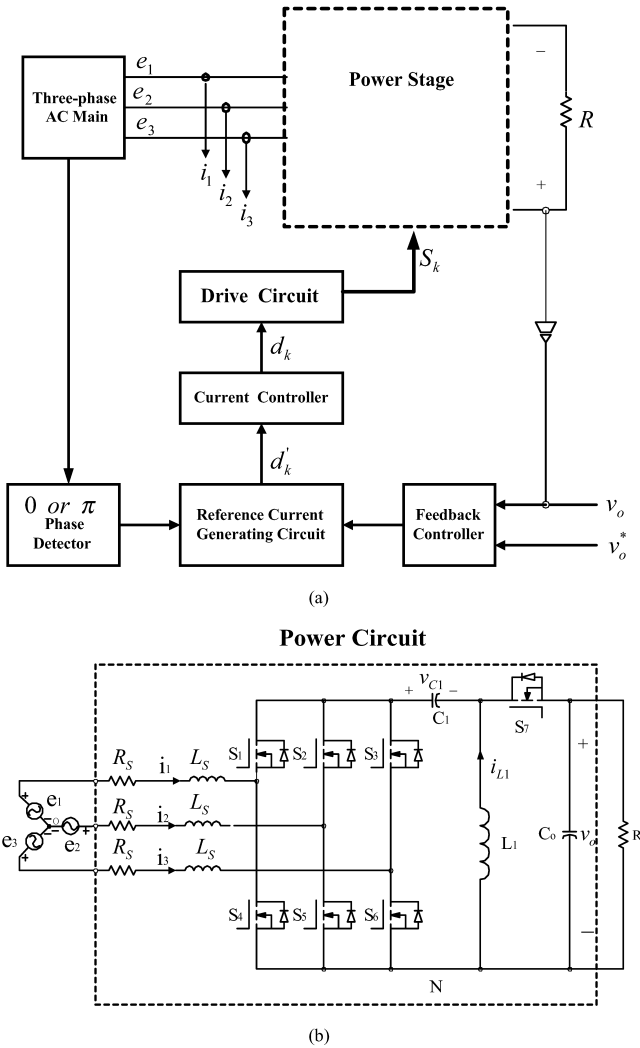


Fig. 1. (a) Block diagram of the proposed switching mode rectifier; (b) The proposed power circuit.

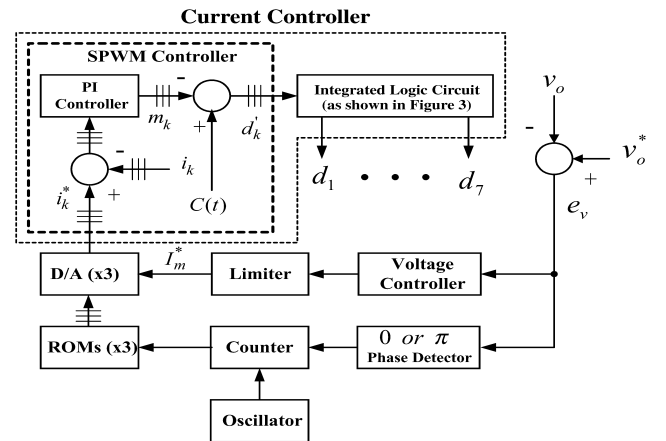


Fig. 2. Block diagram of control strategy.

function basically as that of a boost type converter to charge C_1 and C_o . A more detail discussion of the operation mode with the proposed rectifier will be described in next section.

The second loop is the voltage control loop. The voltage error signal e_v can be obtained by comparing the reference signal v_o^* with the output voltage signal v_o . Hence, a voltage controller, such as the simple proportional integral (PI) controller can be used to shape the system dynamic response performances. In a practical implementation, naturally, a limiter must be used to obtain a reasonable output. This output is then imposed in the current loop to control the magnitude of the current command signals I_m^* . It is obvious that not any multiplier or lock-out circuit (the reason will be described in next section) is used in the proposed control circuit, that can keep minimum cost in the markets.

OPERATION PRINCIPLE

In order to illustrate the operation principle, first, consider the proposed rectifier is operated at rectifier mode. For reference, an ideal three-phase phase voltage waveform is shown in Fig. 5. Since the line currents are controlled to be in phase with the corresponding phase voltages, then none of the input line current in each time

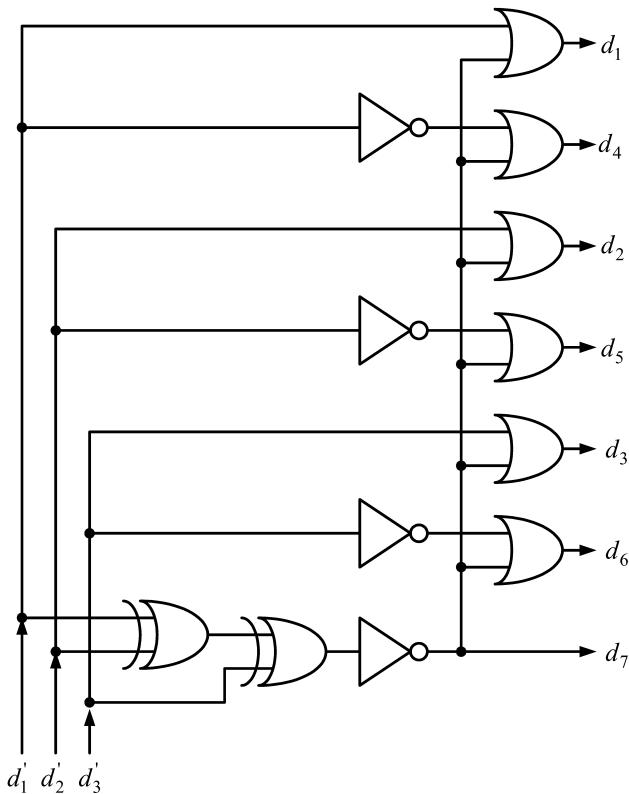


Fig. 3. The proposed logic circuit.

interval changes sign and one current has the largest absolute value with two other currents having smaller magnitude and opposite sign. Here, one take interval B in Fig. 5 as an example. For convenience, one define the following control state flags:

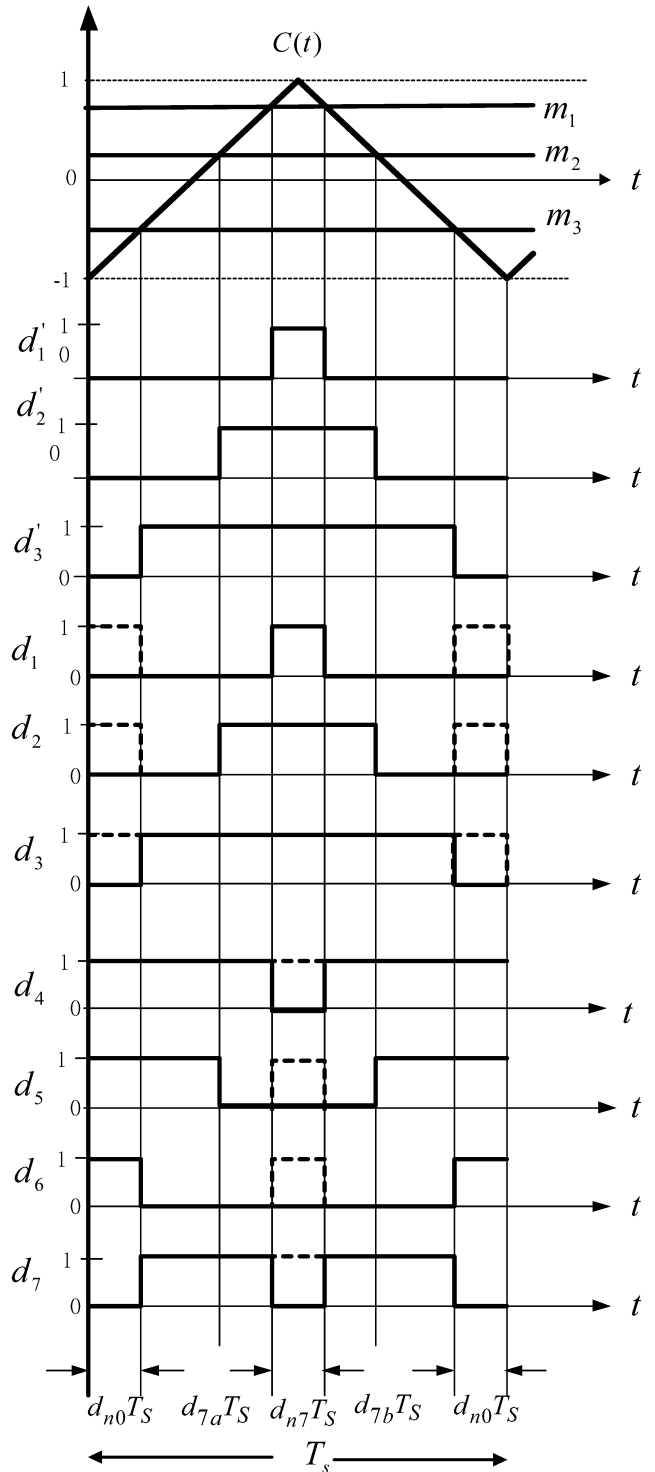


Fig. 4. Pulse patterns generated by proposed PWM scheme.

$$\mu_k(t) \equiv C(t) - m_k(t), \quad k = 1, 2, 3 \quad (1)$$

Hence, one has the following seven modes corresponding to $\mu_k(t)$.

Mode 1: $\mu_1 > 0, \mu_2 > 0, \mu_3 < 0$

This means both currents i_1 and i_2 should be decreased and i_3 should be increased. In this situation, the switches S_1, S_2, S_6, S_7 and S_3, S_4, S_5 should be closed and opened, respectively. Switches S_1 and S_6 are turned on at this situation which shunts the body diode with the MOSFET $R_{ds(on)}$. Switch impedance thus lowers conduction losses. The corresponding equivalent circuit is shown in Fig. 6.

Mode 2: $\mu_1 > 0, \mu_2 < 0, \mu_3 > 0$

This means both currents i_1 and i_3 should be decreased and i_2 should be increased. Similarly, in this situation, the switches S_1, S_3, S_5, S_7 and S_2, S_4, S_6 should be closed and opened, respectively. Due to the limited

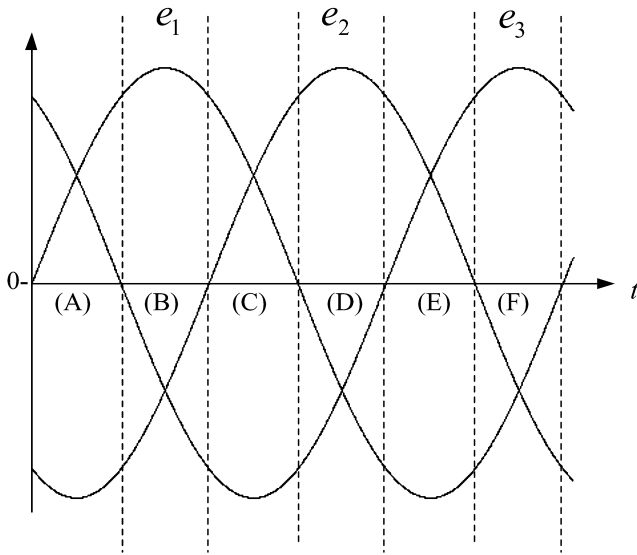


Fig. 5. The ideal three-phase input voltages.

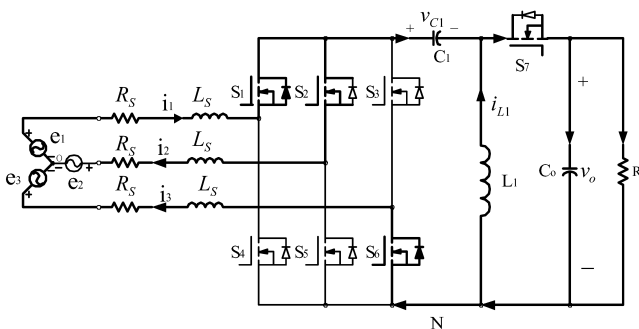


Fig. 6. The equivalent circuit when the proposed is operated at Mode 1.

space, the corresponding equivalent circuit is not shown here.

Mode 3: $\mu_1 > 0, \mu_2 < 0, \mu_3 < 0$

This means currents i_1 should be increased and both i_2 and i_3 should be decreased. Similarly, the switches S_1, S_5, S_6, S_7 and S_2, S_3, S_4 should be closed and opened, respectively. For the purpose of saving space, the resulting equivalent circuit of this mode is not shown here.

Mode 4: $\mu_1 < 0, \mu_2 > 0, \mu_3 > 0$

This means currents i_1 should be increased and both i_2 and i_3 should be decreased. Hence, the switches S_2, S_3, S_4, S_7 and S_1, S_5, S_6 should be closed and opened, respectively. Also, according to the relations of I_m and i_{L1} , there are three different cases (i.e. $I_m > i_{L1}, I_m = i_{L1}$ and $I_m < i_{L1}$) exist. Fig. 7(a)~(c) shows the resulting

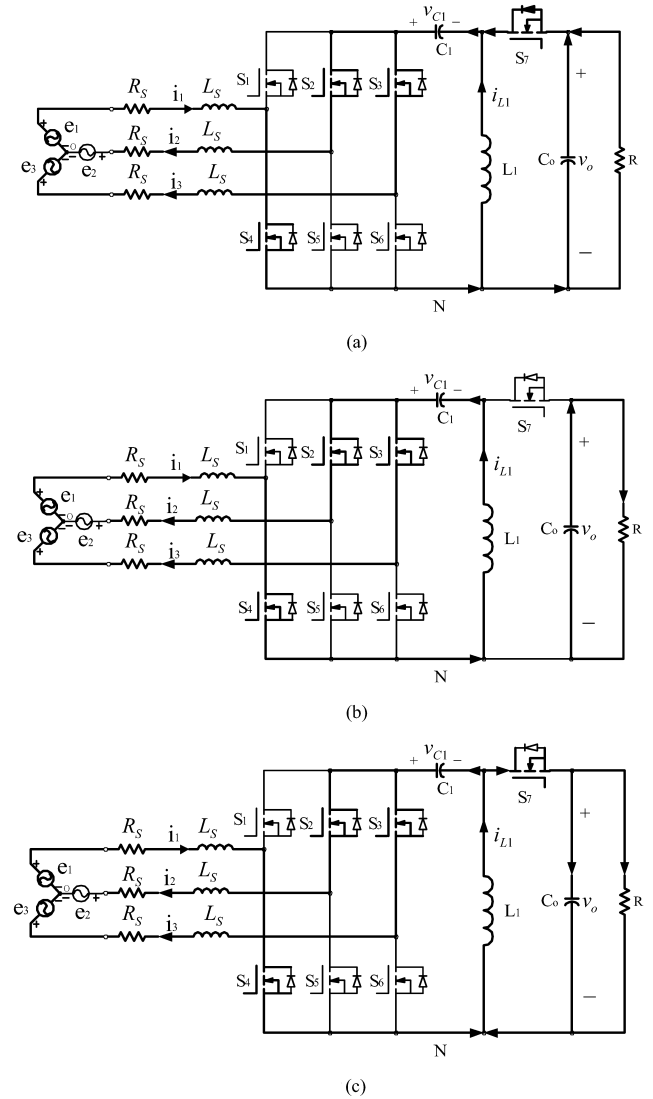


Fig. 7. The equivalent circuit when the proposed is operated at Mode 4 and (a) $I_m > i_{L1}$; (b) $I_m = i_{L1}$; (c) $I_m < i_{L1}$.

equivalent circuit when $I_m > i_{L1}$, $I_m = i_{L1}$ and $I_m < i_{L1}$ correspondingly. As can be observed from Fig. 7, it is interesting to see what the proposed rectifier can be normally operated even when $I_m \leq i_{L1}$. In addition, the anti-parallel diode of S_7 will also be conducted when $I_m > i_{L1}$.

Mode 5: $\mu_1 < 0, \mu_2 > 0, \mu_3 < 0$

This means both currents i_1 and i_3 should be increased and i_2 should be decreased. Switches S_2, S_4, S_6, S_7 and S_1, S_3, S_5 should be closed and opened, respectively. Also, according to the relation of I_m and i_{L1} , three different cases, $I_m > i_{L1}$, $I_m = i_{L1}$ and $I_m < i_{L1}$ will be generated. The resulting circuit of this mode is not shown here in interest of the saving the space.

Mode 6: $\mu_1 < 0, \mu_2 < 0, \mu_3 > 0$

This means both currents i_1 and i_2 should be increased and i_3 should be decreased. Similarly, the switches S_3, S_4, S_5, S_7 and S_1, S_2, S_6 should be closed and opened, respectively. Also, according to the relation of I_m and i_{L1} , three different cases, $I_m > i_{L1}$, $I_m = i_{L1}$ and $I_m < i_{L1}$ will be generated.

Mode 7: $\mu_1 < 0, \mu_2 < 0, \mu_3 < 0$ (or $\mu_1 > 0, \mu_2 > 0, \mu_3 > 0$)

In this mode, to maintain the normal operation principle of the traditional SEPIC DC/DC converter for the DC part of the proposed converter and reduce the conduction losses, the switches $S_1 \sim S_6$ and S_7 should be closed and opened, respectively. The corresponding equivalent circuit is shown in Fig. 8.

Similarly, the selected switches for other intervals of Fig. 5 and regeneration mode can be easily obtained. From the above discussion, one can see that the i_{L1} current is boosted only happen at mode 7 by v_{C1} . Also, practically, by means of the finite turn on/off time of semiconductor devices, it is possible to have a very short time period of short circuit of the bridge arms during mode transitions. In this case, the effect is similar to the mode 7. Hence, the lock-out circuit in conventional power factor regulators can be eliminated in the proposed power correction circuit.

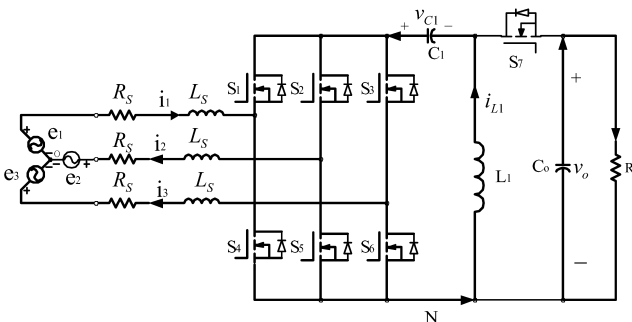


Fig. 8. The equivalent circuit when the proposed is operated at Mode 7.

ACCURATE SIMULATION MODEL

To further explore the accurate simulation model, one can consider the conceptual gating signals of seven switches for one switching cycle. From Figs. 1 and 4 by neglecting the ESR of C_1, C_o and L_1 , using the state space averaging technique[14] one can get the following averaged equation.

$$\begin{bmatrix} \frac{di_1}{dt} \\ \frac{di_2}{dt} \\ \frac{di_3}{dt} \\ \frac{di_{L1}}{dt} \\ \frac{dv_{C1}}{dt} \\ \frac{dv_o}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R_S}{L_S} & 0 & 0 & 0 & -\frac{d_1}{L_S} & -\frac{d_1}{L_S} \\ 0 & -\frac{R_S}{L_S} & 0 & 0 & -\frac{d_2}{L_S} & -\frac{d_2}{L_S} \\ 0 & 0 & -\frac{R_S}{L_S} & 0 & -\frac{d_3}{L_S} & -\frac{d_3}{L_S} \\ 0 & 0 & 0 & 0 & \frac{d_{7a}+d_{7b}}{L_1} & \frac{1-(d_{7a}+d_{7b})}{L_1} \\ \frac{d_1}{C_1} & \frac{d_2}{C_1} & \frac{d_3}{C_1} & \frac{1-(d_{7a}+d_{7b})}{C_1} & 0 & 0 \\ \frac{d_1}{C_o} & \frac{d_2}{C_o} & \frac{d_3}{C_o} & \frac{1-(d_{7a}+d_{7b})}{C_o} & 0 & -\frac{1}{RC_o} \end{bmatrix}$$

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_{L1} \\ v_{C1} \\ v_o \end{bmatrix} + \begin{bmatrix} \frac{e_1 - v_{NO}}{L_S} \\ \frac{e_2 - v_{NO}}{L_S} \\ \frac{e_3 - v_{NO}}{L_S} \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad (2)$$

Assume that

$$e_k = V_m \cos[\omega t - (k-1)120^\circ], i_k = I_m \cos[\omega t - \phi - (k-1)120^\circ], k = 1, 2, 3 \quad (3)$$

where V_m and I_m are the maximum input phase voltage and input line current respectively, and the phase shift ϕ is included for generality.

Substituting (3) into the upper half of equation (2) it is straightforward to get

$$v_{NO} = -\frac{1}{3} \sum_{k=1}^3 d_k (v_{C1} + v_o) \quad (4)$$

The signals of $d'_k, k = 1, 2, 3$ in Fig. 4 are determined by comparing the modulation waves with triangular waves. Hence, with simple geometric calculations one can express d'_k and the total null vector duty ratio d_{nv} as follows:

$$d'_k \equiv \frac{T_k}{T_s} = \frac{1+m_k}{2}, m_k \equiv M \sin[\omega t - \theta - \frac{2\pi(k-1)}{3}]$$

$$k = 1, 2, 3 \quad (5)$$

$$d_{nv} = d_{n0} + d_{n7} \quad (6)$$

where T_S is the switching period, d_{n0} and d_{n7} denote the null space vector [15] duty ratio of V_0 and V_7 respectively as well as M and θ are the modulation index and modulation phase displacement, respectively.

From (6) one can know that the total null vector duty ratio is apportioned between the two null vector duty ratio d_{n0} and d_{n7} . However, each individual null vector duty ratio is still not determined. For convenience, one can define a null vector duty ratio-apportioning factor:

$$\xi = \frac{d_{n0}}{d_{n0} + d_{n7}} \quad (7)$$

Substituting (6) into (7) and considering Fig. 4, one can express d_{n0} and d_{n7} as follows:

$$d_{n0} = \xi(1 + d'_1 - d'_3) \quad (8)$$

$$d_{n7} = d_{nv}(1 - \xi) \quad (9)$$

The above equations are valid for the condition of $m_1 > m_2 > m_3$ but the conclusion can be easily generalized to other cases as following the expressions.

$$\xi = \frac{1 - \text{Min}[m_k]}{2 + \text{Max}[m_k] - \text{Min}[m_k]}, \quad k \in \{1, 2, 3\} \quad (10)$$

$$d_{n0} = \xi(1 + \text{Min}[m_k] - \text{Max}[m_k]) \equiv \frac{1 + m_{n0}}{2}, \quad k \in \{1, 2, 3\} \quad (11)$$

$$d_{n7} = \frac{1 + m_{n7}}{2} \quad (12)$$

where m_{n0} and m_{n7} are the time varying part modulation indices to be decided by the reference wave m_k .

From above results, one can know that the apportioning of null vector duty ratio between two null vectors that represents a degree of freedom that can be used to minimize the input current THD.

Since the conducting states of S_k is determined by d'_k , hence the duty ratio d_k , $k = 1, 2, \dots, 7$ corresponding to the switches S_k can be expressed as follows:

$$d_k = d'_k + d_{n0}, \quad k = 1, 2, 3 \quad (13)$$

$$d_{k+3} = 1 - d'_k + d_{n7}, \quad k = 1, 2, 3 \quad (14)$$

$$d_7 \equiv d_{7a} + d_{7b} = 1 - d_{nv} = \frac{1 - m_7}{2} \quad (15)$$

where m_7 denotes the time varying part modulation index of S_7 and can be decided by substituting (6), (11) and (12) into (15). Thus,

$$m_7 = 1 - \frac{\sqrt{3}}{2} M \cos(\omega t + \frac{\pi}{2} - \psi + j \frac{\pi}{6}), \quad j = 1, 2, \dots, 11 \quad (16a)$$

$$M = \frac{2}{v_{C1}} \{ [V_m - I_m(R_S \cos\phi + \omega L_S \sin\phi)]^2 + [I_m(R_S \sin\phi + \omega L_S \cos\phi)]^2 \}^{1/2}, \quad (16b)$$

$$\phi = \tan^{-1} \frac{I_m(R_S \sin\phi + \omega L_S \cos\phi)}{V_m - I_m(R_S \cos\phi + \omega L_S \sin\phi)} \quad (16c)$$

Then, by substituting (3)-(6), (13) and (15) into (2), one has the following matrix form.

$$\dot{X} = AX + BU, \quad A \equiv \begin{bmatrix} A_1 & A_2 \\ A_3 & A_4 \end{bmatrix} \quad (17)$$

where

$$X = [i_1 \ i_2 \ i_3 \ i_{L1} \ v_{C1} \ v_o]^T \quad (18)$$

$$A_1 = -\frac{R_S}{L_S} [I] \quad (19)$$

$$A_2 = -\frac{1}{2L_S} \begin{bmatrix} 0 & m_1 & m_1 \\ 0 & m_2 & m_2 \\ 0 & m_3 & m_3 \end{bmatrix} \quad (20)$$

$$A_3 = -\frac{L_S}{C_1} A_2^T \quad (21)$$

$$A_4 = \begin{bmatrix} 0 & \frac{d_{nv}}{L_1} & \frac{1 - d_{nv}}{L_1} \\ -\frac{d_{nv}}{C_1} & 0 & 0 \\ \frac{1 - d_{nv}}{C_0} & 0 & \frac{-1}{C_0 R} \end{bmatrix} \quad (22)$$

$$B = \begin{bmatrix} I \\ 0 \end{bmatrix} \quad (23)$$

$$U = [e_1 \ e_2 \ e_3]^T \quad (24)$$

and $[I]$ denotes the unity matrix.

The above expression can be used to provide a convenient numerical simulation tool such as MATLAB for the proposed rectifier. Figs. 9 and 10 show some simulated results. It is observed from Figs. 9 and 10 that the proposed converter not only has both step-up/down and regeneration capability but also clean sinusoidal input currents and unity power factor, as well as clean DC voltage. It may be worth mentioning what for a desired output voltage, the duty cycle of d_{n0} and d_{n7} can be uniquely determined by m_k . To avoid explicit calculation of m_k and achieve adjustable output DC voltage, a closed loop output voltage control is adopted in hard-

ware implementation as shown in Fig. 2.

In addition, substituting (13)-(16) into (17) and under steady state, one can obtain the following relation:

$$V_{C1} = \frac{1-d_{nv}}{d_{nv}} V_o \tag{25}$$

$$V_o = \left[\frac{3}{2} I_m^* R (V_m \cos\phi - I_m^* R_s) \right]^{\frac{1}{2}} \tag{26}$$

Form (6) , (25) and (26), it is interesting to see that V_{C1} is not constant, however the output voltage V_o is indeed constant DC as expected. In fact, (26) actually represents the principle of conservation of power.

SOME EXPERIMENTAL RESULTS

To facilitate the understanding of the above theo-

retical results and as verification, a prototype hardware circuit is constructed. The parameters of the rectifier in Fig. 1 are listed below for reference.

$$L_s = 6\text{mH}, R_s = 0.41\Omega, \omega = 377\text{rad/sec},$$

$$L_1 = 3.25\text{mH}, C_o = 2200\mu\text{F}, C_1 = 470\mu\text{F},$$

Power switches $S_1 \sim S_7$: IRF460.

The switching frequency for the proposed rectifier is selected to be 3kHz. Fig. 11 shows the input current and voltage waveforms when the proposed rectifier is operated at step-up mode. To show the step-down capability of the proposed rectifier, the waveforms of the input current and output voltage are shown in Fig. 12. The spectrum of input line current waveform is also

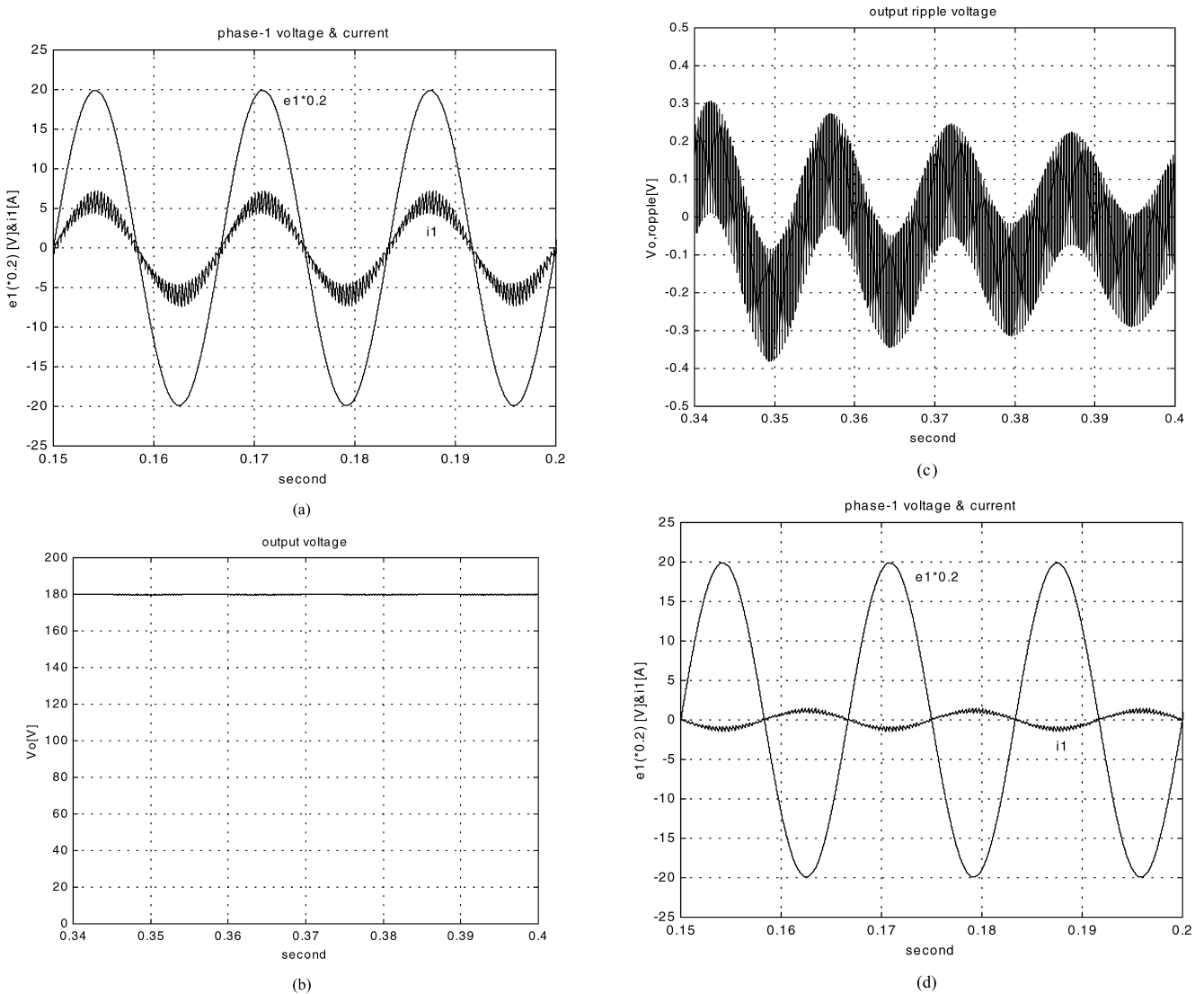


Fig. 9. Simulated input current and output voltage waveforms for step-up mode. (a) Phase-1 input current and voltage; (b) DC output voltage; (c) Output ripples voltage; (d) Phase-1 input current and voltage for regenerative mode.

shown for reference. As can be observed from Figs. 11 and 12 that the results are very nice agreement with the simulation and theoretical results as shown in Figs. 9 and 10, respectively as expected.

CONCLUSIONS

In this paper, based on the null space vector duty cycle control a novel three-phase switching mode interface with its control circuit is proposed. The proposed rectifier can achieve the desired qualities such as clean sinusoidal input current, unity power factor, bidirectional power flow, step up/down output dc voltage and insensitive to input voltage. Also, the proposed control

circuit does not use of multiplier and lock-out circuit implemented in conventional power correction rectifiers that can keep minimum cost in the markets. An accurate simulation model is also presented which can be used for convenient simulation with common PC software tools. Finally, some simulation and experimental results are presented for verification the validity of the proposed rectifier.

ACKNOWLEDGMENT

The author gratefully thanks the financial support of the National Science Council of Taiwan, R.O.C. through grant number NSC 90-2213-E-233-003.

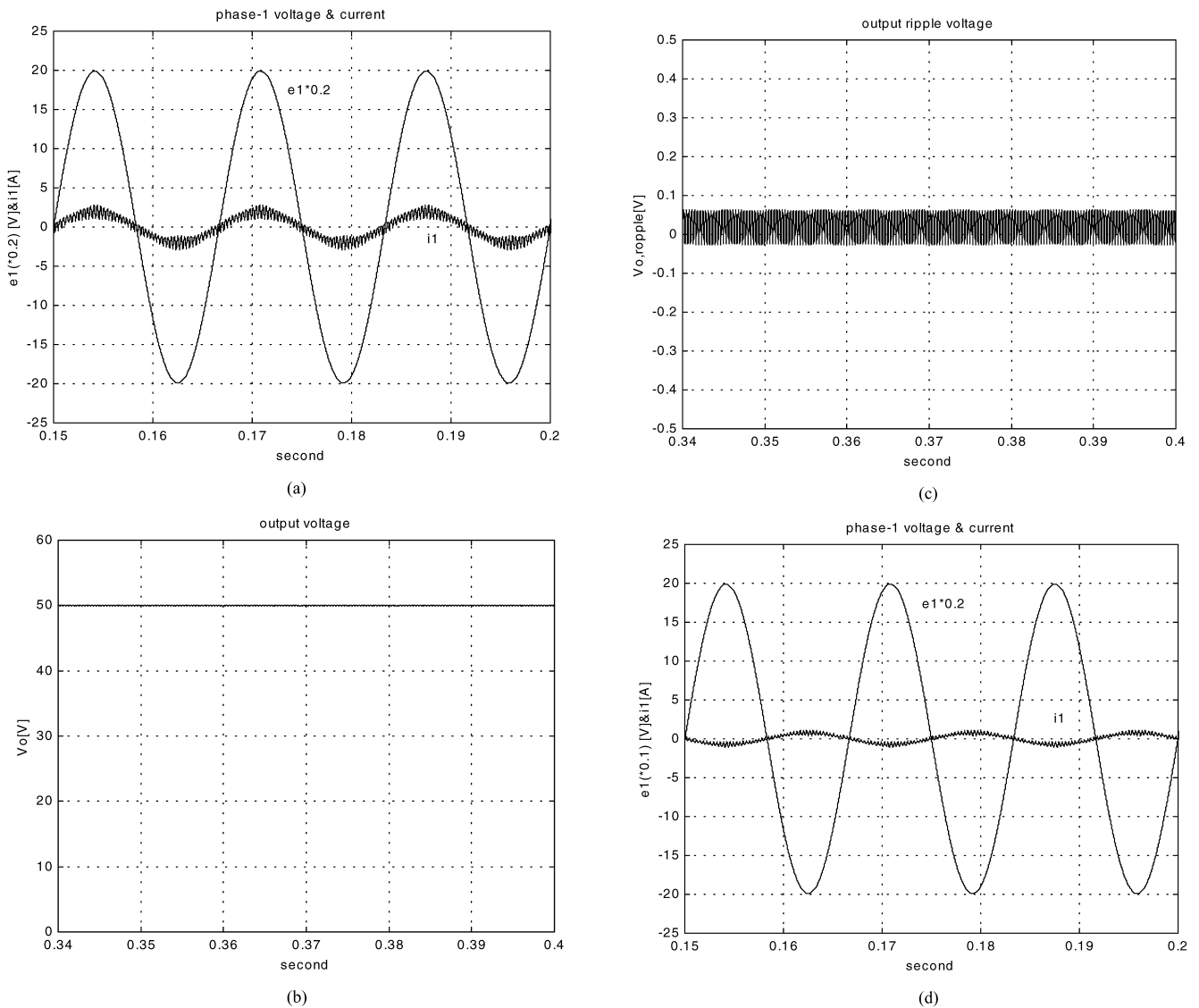
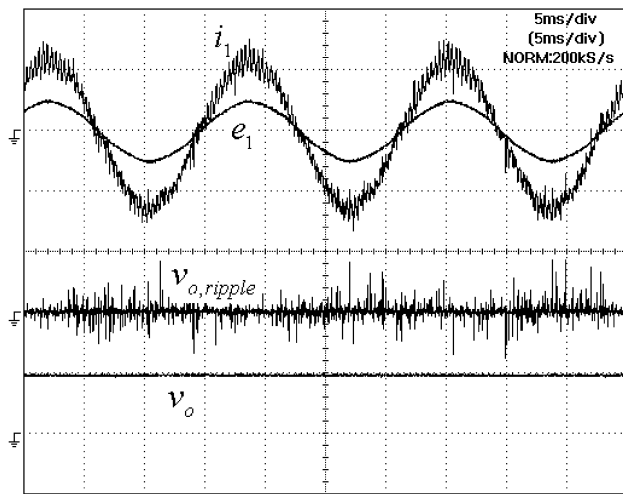
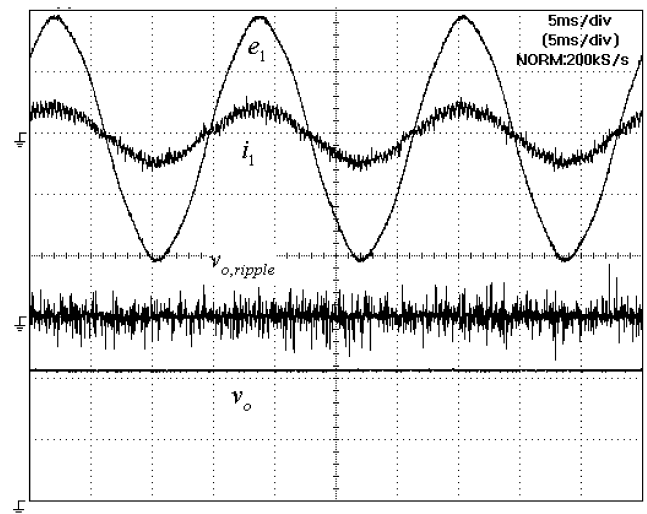


Fig. 10. Simulated input current and output voltage waveforms for step-down mode. (a) Phase-1 input current and voltage. (b) DC output voltage. (c) Output ripples voltage. (d) Phase-1 input current and voltage for regenerative mode.



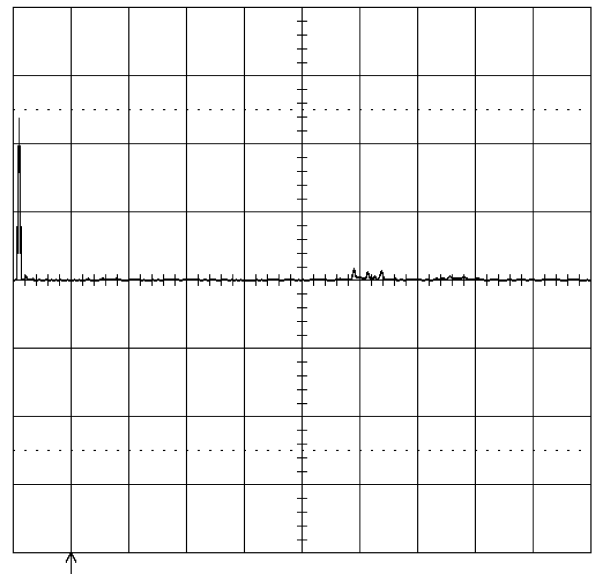
($v_{o,ripple}$:2V/div, v_o :50V/div; e_1 :200V/div; i_1 :5A/div)

Fig. 11. Measured input and output waveforms for step-down mode.



($v_{o,ripple}$:2V/div; v_o :75V/div; e_1 :50V/div; i_1 :5A/div)

(a)



(1A/div, 500Hz/div)

(b)

Fig. 12. (a) Measured input and output waveforms for step-up mode; (b) Measured spectrum of the line current waveform.

REFERENCES

1. Duffey, C.K. and Stratford, R.P., "Update of Harmonic Standard IEEE-519: IEEE Recommended Practices and Requirements for Harmonic Control in Electric Power Systems," *IEEE Transactions on Industry Applications*, Vol. 25, No. 6, pp. 1025-1034 (1989).
2. Mohon, N., Undeland, T.M. and Robbins, W.P., *Power Electronics: Converters, Applications and Design*, Canada: John Wiley and Sons (1989).
3. Andrieu, Ch., Ferrieux, J-P. and Rocher, M., "The AC/DC Stage: A Survey of the Structures and Chopper Control Modes for Power Factor Correction," *EPE Journal*, Vol. 5, pp. 17-22 (1996).
4. Mao, H., Lee, F.C., Jiang, Y. and Borojevic, D., "Review of Power Factor Correction Techniques," Proceedings of the 2nd International Power Electronics and Motion Control Conference (IMEPC'97 Record), Hangzhou, China, pp. 9-21 (1997).
5. Mao, H., Lee, F.C., Borojevic, D. and Hiti, S., "Review of High-Performance Three-Phase Power-Factor Correction Circuits," *IEEE Transactions on Industry Electronics*, Vol. 44, No. 4, pp. 437-446 (1997).
6. Yasuyuki, N., Akeshi, M. and Hideo, T., "A New Instantaneous-Current Controller for Three-Phase Buck-Boost and Buck Converters with PFC Operations," *IEEE Applied Power Electronics Conference and Exposition (APEC'95 Record)*, Dallas, TX, USA, pp. 875-883 (1995).
7. Itoh, R. and Ishizaka, K., "Three-phase Flyback AC-DC Converter with Sinusoidal Supply Currents," *IEE Proceedings, Part B*, Vol. 138, No. 3, pp. 143-151 (1991).
8. Johann, W., Hari, S. and Uwe, D., "A Novel Three-Phase

9. Jacobs, M.E., Jaiang, Y. and Mao, H., "Phase Selection Circuit for Three Phase Power Converter and Method of Operation Thereof," US Patent, No. 6046915 (2000).
10. Strand, T. and Littlefair, M.J., "Power Factor Cor-

Three-Switch Three-Level High Power Factor SEPIC-type AC-to-DC Converter," *IEEE Applied Power Electronics Conference and Exposition (APEC'97 Record)*, Atlanta, GA, USA, pp. 657-665 (1997).

- rector," US Patent, No. 0036094 A1 (2001).
11. Dixon, L., "High Power Factor Preregulator Using the SEPIC Converter," Unitorde Power Supply Design Seminar, SEM-900 (1993).
 12. Koerner, M., "Recent Developments in Aircraft Emergency Power," *Energy Conversion Engineering Conference and Exhibit (IECE'35 Record)*, Las Vegas, NV, USA, pp. 12 -19(2000).
 13. Lai, Z. and Smedley, K.M., "A Single-Stage Power-Factor-Corrected AC-DC Converter with Fast Output Regulation and Improved Current Shaping," *High Power Conversion Proceedings*, pp. 51-62 (1997).
 14. Middlebrook, R.D. and Cuk, S.M., "A General Unified Approach to Modelling Switching Convertor Power Stages," *IEEE Power Electronics Specialists Conference (PESC'76 Record)*, Cleveland, OH, USA, pp. 18-34 (1976).
 15. Lee, D.C. and Lee, G.M., "A Novel Overmodulation Technique for Space Vector PWM Inverters," *IEEE Power Electronics Specialists Conference (PESC'97 Record)*, Gateway, ST, USA, pp. 1014-1019 (1997).