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Recommended Citation

Li, Jung-Chien and Chen, Han-Yang (2004) "Discontinuous Conduction Mode of Negative Output Elementary Circuit,"
Journal of Marine Science and Technology. Vol. 12: Iss. 2, Article 8.

DOI: 10.51400/2709-6998.2229

Available at: <https://jmstt.ntou.edu.tw/journal/vol12/iss2/8>

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Short Paper

DISCONTINUOUS CONDUCTION MODE OF NEGATIVE OUTPUT ELEMENTARY CIRCUIT

Jung-Chien Li* and Han-Yang Chen**

Key words: Negative output, discontinuous conduction mode.

ABSTRACT

The negative output elementary circuit operated in the discontinuous conduction mode is discussed. The voltage transfer gain of this dc-to-dc converter depends on switching frequency, conduction duty ratio, inductance, and load resistance. The condition for the discontinuous conduction mode is derived and verified. The variation ratio of the output voltage is also derived.

I. INTRODUCTION

The voltage lift technique is a popular method employed in the design of dc-to-dc converters. It can be used to design high voltage gain converters. The negative output super-lift converters operated in the continuous conduction mode (CCM) were proposed in [1]. The positive output super-lift converters operated in the CCM were proposed in [2]. The first stage of the negative output super-lift converter is called the elementary circuit, where only one inductor exists.

The operating of the negative output elementary circuit can be classified as the CCM [1] and the discontinuous conduction mode (DCM). In the CCM, the inductor current waveform is continuous. In the DCM, the inductor current waveform is discontinuous. We investigate the DCM of the negative output (N/O) elementary circuit in this paper.

II. STEADY-STATE ANALYSIS

The discontinuous operation of the N/O elementary circuit is shown in Fig. 1, where the inductor current waveform is shown in Fig. 2. The capacitance

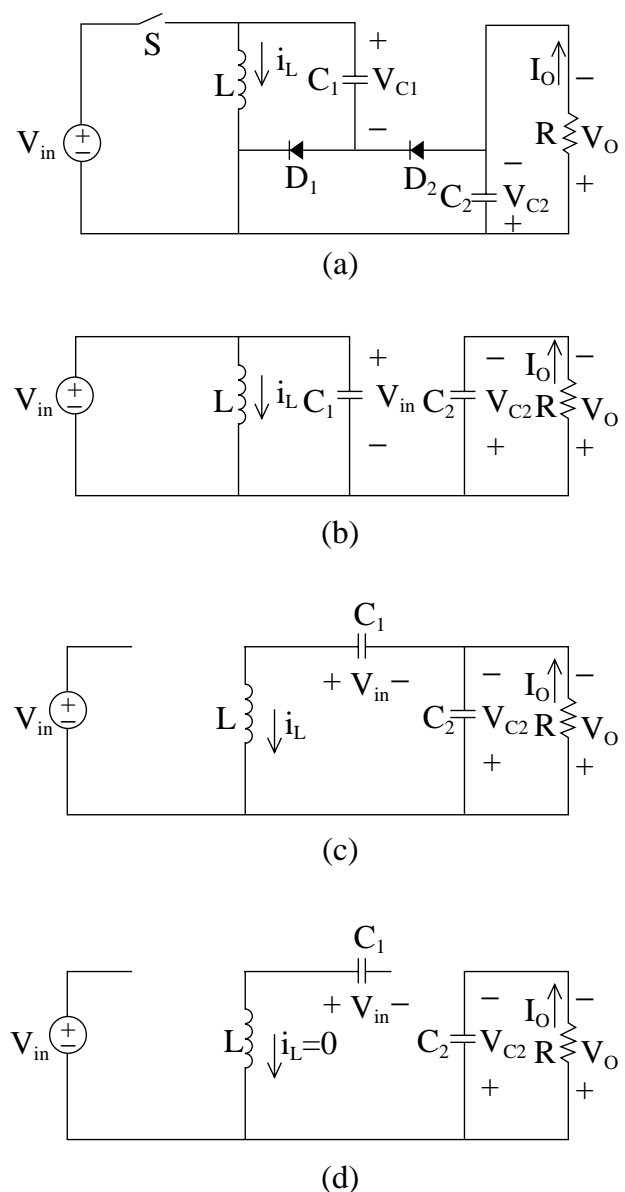


Fig. 1. N/O elementary circuit operated in the DCM (a) Circuit diagram (b) Equivalent circuit during switching-on (D_1 on, D_2 off) (c) Equivalent circuit during switching-off (D_1 off, D_2 on) (d) Equivalent circuit during switching-off (D_1 off, D_2 off).

Paper Submitted 02/23/04, Accepted 05/04/04. Author for Correspondence: Jung-Chien Li. E-mail: B0088@mail.ntou.edu.tw.

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values are large enough that the capacitor voltages can be assumed to be constant.

Consider Fig. 2, where the switching period is T (and hence the switching frequency is $f = 1/T$) and the conduction duty ratio is k . During $0 \leq t \leq kT$, the equivalent circuit is Fig. 1(b), where the inductor current i_L is increasing. During $kT \leq t \leq (k + k')T$, the equivalent circuit is Fig. 1(c), where the inductor current i_L is decreasing. During $(k + k')T \leq t \leq T$, the equivalent circuit is Fig. 1(d), where the inductor current i_L is zero. It can be observed from Fig. 2 that the DCM condition is

$$k + k' < 1 \quad (1)$$

Consider Fig. 1(b), (c) and Fig. 2. During $0 \leq t \leq kT$, i_L increases with slope V_{in}/L . During $kT \leq t \leq (k + k')T$, i_L decreases with slope $-(V_o - V_{in})/L$. Therefore,

$$\Delta i_L = \frac{V_{in}}{L} kT = \frac{V_o - V_{in}}{L} k'T \quad (2)$$

Equation (2) can be simplified as

$$kV_{in} = k'(V_o - V_{in}) \quad (3)$$

In the steady state, the average capacitor current is zero. Considering the current flowing through the capacitor C_2 in Fig. 1(b), (c), (d), we have

$$k'T \left(\frac{1}{2} \Delta i_L - I_o \right) = kTI_o + (1 - k - k')TI_o = (1 - k')TI_o \quad (4)$$

Using $\Delta i_L = (V_{in}/L)kT$ [from (2)], $I_o = V_o/R$ (where R is the load resistance), and $T = 1/f$ in (4), we obtain

$$\frac{1}{2} \frac{V_{in} k k'}{L f} = \frac{V_o}{R} \quad (5)$$

Combining (3) and (5), we obtain

$$k' = \frac{kV_{in}}{V_o - V_{in}} = \frac{2LfV_o}{V_{in}kR} \quad (6)$$

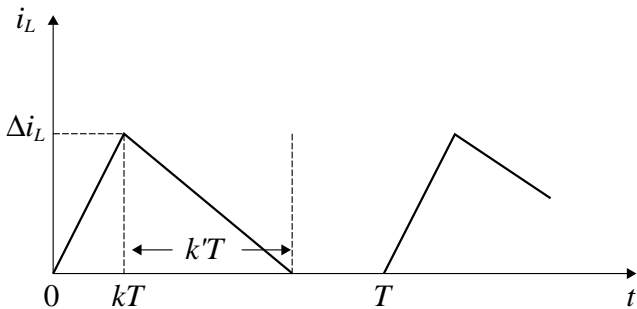


Fig. 2. Discontinuous inductor current waveform.

We define the voltage transfer gain $G = V_o/V_{in}$ in (6) and obtain

$$k' = \frac{k}{G - 1} = \frac{2LfG}{kR} \quad (7)$$

Therefore,

$$G^2 - G - \frac{k^2 R}{2Lf} = 0 \quad (8)$$

Solving (8), we obtain the voltage transfer gain as

$$G = \frac{1}{2} \left(1 + \sqrt{1 + 2k^2 \frac{R}{Lf}} \right) \quad (9)$$

III. DCM CONDITION AND ITS VERIFICATION

The DCM condition is shown in (1), where $k' = k/(G - 1)$ [from (7)]. Therefore,

$$\begin{aligned} k + \frac{k}{G - 1} < 1 &\Rightarrow \frac{k}{G - 1} < 1 - k \Rightarrow \frac{G - 1}{k} > \frac{1}{1 - k} \\ &\Rightarrow G - 1 > \frac{k}{1 - k} \Rightarrow G > 1 + \frac{k}{1 - k} \Rightarrow G > \frac{1}{1 - k} \end{aligned} \quad (10)$$

Substituting (9) into (10), we obtain

$$\begin{aligned} 1 + \sqrt{1 + 2k^2 \frac{R}{Lf}} > \frac{2}{1 - k} &\Rightarrow 1 + 2k^2 \frac{R}{Lf} > \left(\frac{2}{1 - k} - 1 \right)^2 \\ &= \left(\frac{1 + k}{1 - k} \right)^2 \Rightarrow 2k^2 \frac{R}{fL} > \left(\frac{1 + k}{1 - k} \right)^2 - 1 = \frac{4k}{(1 - k)^2} \\ &\Rightarrow \frac{R}{fL} > \frac{2}{k(1 - k)^2} \end{aligned} \quad (11)$$

Equation (11) is the DCM condition, which can be verified from [1] as follows. Reference [1] gave the variation ratio of the inductor current i_L (in the CCM) as

$$\xi = \frac{\Delta i_L / 2}{I_L} = k(1 - k)^2 \frac{R}{2fL} \quad (12)$$

where $\xi < 1$ in the CCM and $\xi > 1$ in the DCM. Then the DCM condition is

$$k(1 - k)^2 \frac{R}{2fL} > 1 \Rightarrow \frac{R}{fL} > \frac{2}{k(1 - k)^2} \quad (13)$$

which agrees with (11).

Both (11) and (13) can be rewritten as

$$\frac{fL}{R} < g(k) \quad (14)$$

where

$$g(k) = \frac{1}{2} k(1 - k)^2 \quad (15)$$

for which $0 < k < 1$. The maximum value of $g(k)$ can be derived as follows.

$$g'(k) = \frac{1}{2}(3k^2 - 4k + 1) = 0 \Rightarrow k = \frac{1}{3} \Rightarrow g_{\max}(k) = g\left(\frac{1}{3}\right) = \frac{2}{27}$$

Therefore, (14) can be illustrated in Fig. 3, where $k_1 < k < k_2$ corresponds to the DCM. However, if $\frac{fL}{R} > \frac{2}{27}$, then the converter always operates in the CCM.

IV. VARIATION RATIOS OF THE CAPACITOR VOLTAGES

The peak to peak ripple voltage of the output voltage v_o (which is also the capacitor voltage v_{c2}) is [from Fig. 1(b) and Fig. 1(d)]

$$\Delta v_o = \frac{\Delta Q}{C_2} = \frac{I_o k T + I_o(1 - k - k') T}{C_2} = \frac{I_o(1 - k') T}{C_2} = \frac{V_o(1 - k')}{f R C_2} \tag{16}$$

Therefore, the variation ratio of the output voltage v_o is

$$\epsilon = \frac{\Delta v_o / 2}{V_o} = \frac{1 - k'}{2 f R C_2} \tag{17}$$

where [using (7) and (9)]

$$1 - k' = 1 - \frac{2 L f G}{k R} = 1 - \frac{L f}{k R} \left(1 + \sqrt{1 + 2 k^2 \frac{R}{L f}}\right) \tag{18}$$

The peak to peak ripple voltage of the capacitor C_1 is [from Fig. 1(c), Fig. 2, and (2)]

$$\Delta v_{c1} = \frac{\Delta Q_1}{C_1} = \frac{1}{C_1} \times \frac{1}{2} \Delta i_L \times k T = \frac{1}{C_1} \times \frac{1}{2} \frac{V_{in}}{L} k T \times k T \tag{19}$$

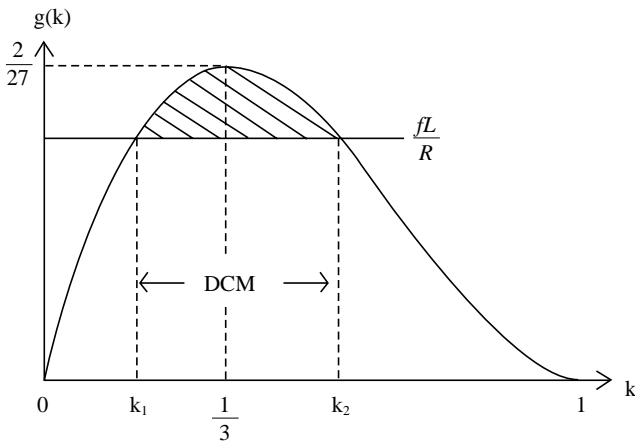


Fig. 3. Illustration of (14).

Since $V_{c1} = V_{in}$ [from Fig. 1(b)], the variation ratio of the capacitor voltage v_{c1} is [using (7) and (9)]

$$\epsilon_1 = \frac{\Delta v_{c1} / 2}{V_{c1}} = \frac{\Delta v_{c1}}{2 V_{in}} = \frac{k k'}{4 L C_1 f^2} = \frac{k}{4 L C_1 f^2} \frac{2 L f G}{k R} = \frac{G}{2 C_1 f R} = \frac{1}{4 C_1 f R} \left(1 + \sqrt{1 + 2 k^2 \frac{R}{L f}}\right) \tag{20}$$

V. SIMULATION AND EXPERIMENTAL RESULTS

We choose $V_{in} = 10V$, $L = 45 \mu H$, $R = 416.6 \Omega$, $C_1 = 4.7 \mu F$, $C_2 = 22 \mu F$, $f = 100 \text{ kHz}$, and $k = 0.2$ for the circuit of Fig. 1(a). IsSpice simulation package and

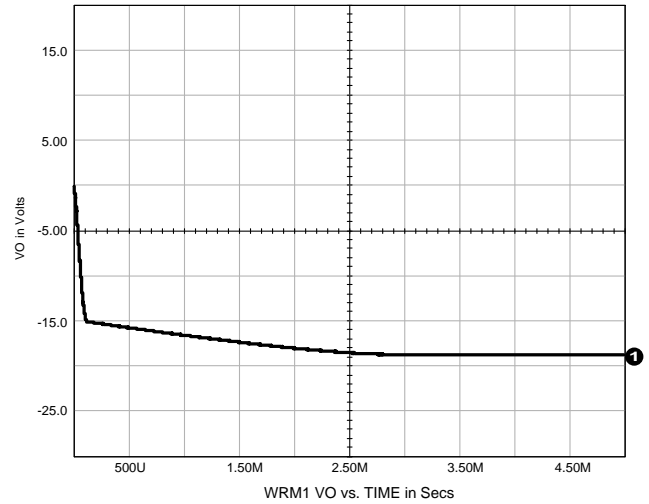


Fig. 4. Simulation result of the output voltage .

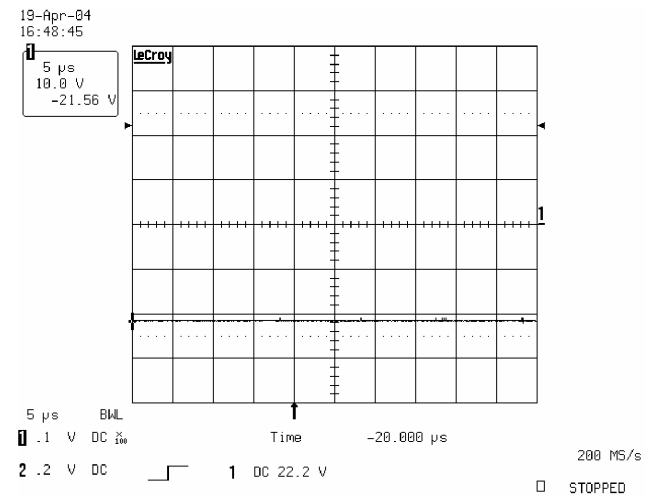


Fig. 5. Experimental result of the output voltage (time: 5 μs/div, voltage: 10 V/div).

LeCroy oscilloscope were applied to the circuit. The simulation and experimental results of the output voltage are shown in Fig. 4 and Fig. 5, respectively. The reader can check that both the simulation and experimental results agree with the analytical result of (9).

VI. CONCLUSIONS

We have derived the voltage transfer gain for the negative output elementary circuit operated in the discontinuous conduction mode. Condition for the discontinuous conduction mode has been derived and verified. The converter can operate in the continuous conduction mode for any conduction duty ratio if the switching frequency or inductance is too large, or if the load resistance is too small. The variation ratios of the capacitor voltages have also been derived, and the corresponding capacitance value can be appropriately selected.

NOMENCLATURE

k conduction duty ratio

T	switching period
f	switching frequency
V_{in}	input voltage
V_o	output voltage
I_o	output current
L	inductance
i_L	inductor current
R	load resistance
G	voltage transfer gain
C_1	input capacitor
C_2	output capacitor
ε	variation ratio of the output voltage
ε_1	variation ratio of the voltage across the capacitor C_1

REFERENCES

1. Luo, F.L. and Ye, H., "Negative Output Super-Lift Converters," *IEEE Trans. Power Electron.*, Vol. 18, No. 5, pp. 1113-1121 (2003).
2. Luo, F.L. and Ye, H., "Positive Output Super-Lift Converters," *IEEE Trans. Power Electron.*, Vol. 18, No. 1, pp. 105-113 (2003).