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DESIGN AND IMPLEMENTATION OF A LOW-VOLTAGE 2.4-GHZ CMOS RF RECEIVER FRONT-END FOR WIRELESS COMMUNICATION

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Key words: receiver, low-voltage, radio frequency (RF), band pass filter (BPF).

ABSTRACT

This paper presents the design of a 1.5 V CMOS RF receiver front-end system which contains a low noise amplifier (LNA) with band pass filter and a down conversion mixer. An inter-stage matching network is added between the common-source and common-gate transistors in the LNA's first stage to further lower the noise and enhance the overall gain. An inductor is used in this inter-stage matching network because of the extra capacitive of MOSFETs in the LNA. The maximum gain achieved of this LNA is 15 dB. The single square-law structure was implemented for this low power consumption and high linearity mixer. From the measured results, the whole receiver provides a conversion gain of 8.5 dB at 2.4 GHz with LO power input -3.5 dBm. The power dissipation of this front-end is 9 mW .

INTRODUCTION

The demand for wireless communications such as cellular phones, wireless local area networks, radio frequency identification (RFID) *etc*. grows quickly recently. The growing wireless communication market has also generated increasing interest in RF technologies. New technologies are developed to increase higher data rates and capacity, and to reduce the power dissipation for longer operation time. Low-voltage and low-power RF circuit design becomes a necessary requirements. This paper describes the design and implementation of a low-voltage and low-power 2.4 GHz CMOS receiver front-end for wireless local area network applications. A block diagram of the heterodyne receiver front- end [6] is shown in Figure 1. The first component in the receiver front-end is the band pass filter (BPF). The major function of this BPF is to contribute the image signal rejection by removing out of band noise. Following the LNA [1-5], the desired signal (RF) of 2.4 GHz down converts to an intermediate frequency (IF) of 100 MHz modulated by a 2.3 GHz local oscillator.

Following text is divided into four parts. Section II describes the circuit analysis. Section III describes the circuit implementation. Section IV gives the measured results. Section V presents the conclusions.

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CIRCUIT ANALYSIS

1. Low noise amplifier

The low noise amplifier is an important block in wireless receivers. It determines the receiver performance. The LNA design is full of trade-offs between optimum gain, optimum input matching, low power consumption, lowest noise figure (NF) and high linearity. In other words, the gain should be high enough to reduce the noise contribution of the subsequent stages, but not so high as to overdrive the subsequent mixer. Secondly, the noise, of course, must be as low as possible to minimize the impact on the receiver noise performance. Thirdly, because the inter-modulation of the two signals in the adjacent channels may appear in the desired channel, which degrades the signal-to-noise ratio, the linearity of a LNA must be high. Furthermore, the input impedance of the LNA must match the characteristic

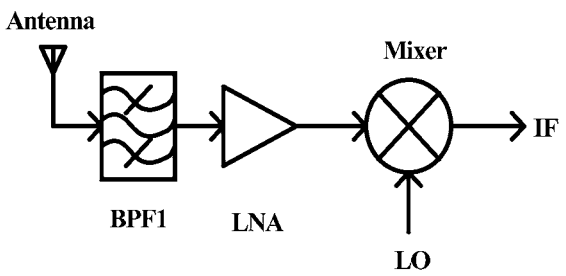

Fig. 1. The RF front-end of the heterodyne receiver.

antenna impedance, such as 50 Ω.

Figure 2 shows the complete LNA. The first stage of the LNA is implemented using a cascode amplifying circuit. In the LNA input stage, inductive source degeneration is used to simultaneously provide the impedance, noise and power gain match. A simple analysis of the input impedance shows that

$$Z_{in} = s(L_g + L_s) + \frac{1}{sC_{gs}} + \frac{1}{sC_i} + \left(\frac{g_m}{C_{gs}}\right)L_S \qquad (1)$$

From Eq. (1) we see that if the input circuit works at series resonance, the input impedance will be purely real impedance and proportional to *Ls*. Hence, the inductance *Ls* is chosen to provide a 50 Ω input impedance at resonance frequency.

The noise figure for the LNA can be computed using [7].

$$F = 1 + \frac{\gamma\omega_0 L}{3v_{sat}} P(\rho, P_D) \qquad (2)$$

$$P(\rho, P_D) \approx \frac{\frac{P_D}{P_0}(1+\frac{\delta}{5\gamma}) + 2|c|\sqrt{\frac{\delta}{5\gamma}}\rho^2 + \frac{P_0}{P_D}\frac{\delta}{5\gamma}\rho^4}{\rho^3} \qquad (3)$$

With the assumption that $\rho << 1$ and $Q_L = \frac{P_0}{P_D}\frac{\rho^2}{1+\rho}$. By employing Eq. (2), we find a value for $Q_{L,\,opt,\,P_D}$ that is the Q_L for a fixed value of P_D where the noise figure is minimal. The LNA input stage can be determined through this method. Most importantly, an inter-stage matching inductor (L_m) is added between the common source transistor and common gate transistor in the LNA's first stage. To simplify the analysis, we can consider a first-order small-signal device model shown in Figure 3. From Figure 3, the output impedance of the common-source stage without L_m can be written as

$$Z_{out1} = \frac{1}{sC_{ds1}} + \frac{g_{m1}}{C_{ds1}}L_S \qquad (4)$$

The input impedance of the common-gate stage can be given by

$$Z_L = \frac{1}{g_{m2} + sC_{gs2}} \qquad (5)$$

Looking at Eqs. (4) and (5) we know that the traditional cascode LNA design did not consider matching the common-source stage and common-gate stage. Without proper matching, the power loss directly degrades the performance of the power gain and the signal-to-noise ratio. By adding the additional matching inductor (L_m), the output impedance of the common-source stage with Lm can be modified such that

$$Z_{out} = sL_m + \frac{1}{sC_{ds1}} + \frac{g_{m1}}{C_{ds1}}L_S \qquad (6)$$

2. Down-conversion mixer

The down-conversion Mixer [6, 8] is used to perform the frequency translation from RF to the base band. The Mixer design forces the same compromises as the LNA. A strong correlation exists among the conversion gain, noise figure, linearity, port-to-port isolation, LO input power and total mixer power. Because the receiver gain can be supported by the LNA, high conversion gain for the Mixer is not often needed. We should tune the conversion gain (CG) to an acceptable value and make the linearity as high as possible for compensation. The LO power must be low enough that can be reduced to insignificant levels of EMI. In Figure 4 we demonstrate a single ended input and output mixer.

The mixer processes the function that converts RF signals into IF signals. The output of a mixer is the product of these two input signals, RF and LO. Assume that two input signals are referred to as V_1 to V_2 in Eqs. (6) and (7).

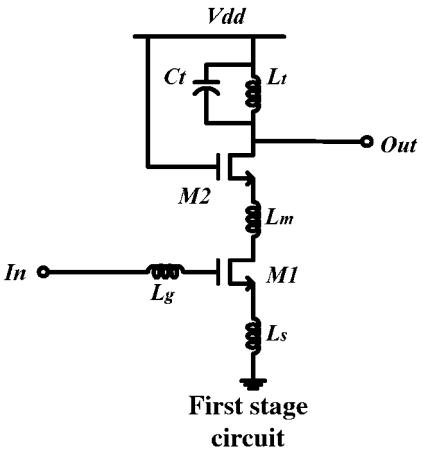

Fig. 2. The LNA circuit cascode stage.

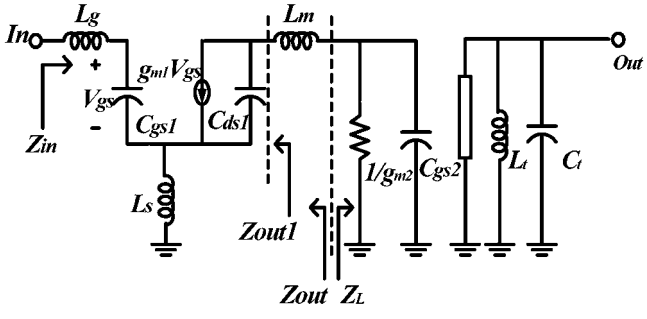

Fig. 3. The equivalent first stage small signal circuit with inter-stage matching inductor.

$$V_1 = A_1 \sin(\omega_1 t) \quad (7)$$

$$V_2 = A_2 \sin(\omega_2 t) \quad (8)$$

The output is according to the (7) and (8) as following:

$$V_o = V_1 V_2$$

$$= A_1 A_2 [\cos(\omega_1 - \omega_2)t - \cos(\omega_1 + \omega_2)t]/2 \quad (9)$$

The result of the output contains two parts, the sum and different frequencies of input signals V_1 and V_2. The sum signal is not the desired signal in the down-conversion processing and must be filtered out by the low pass filter.

The mixer core is comprised of M2, used to commutate the RF signals. It is significant to make the mixer core operation as good as a switch. In other words, the operating point (Q) for M2 must be biased in the saturation region and as close to the triode region as possible. Again, the LO drive must be large enough, but not excessive, to promise steady switching. The mixer actually behaves as a multiplier to sample the RF signals. Figure 4 is a square-law MOSFET mixer. The RF and local oscillator (LO) signals go into the source and gate of the M2. The LO signal input is assumed to be a square wave that is expanded as a Fourier series.

$$V_{LO}(t) = 4[\sin(\omega_{LO}t) + \sin(3\omega_{LO}t)/3 + ...]/\pi \quad (10)$$

then define RF current

$$I_{RF}(t) = V_{RF}(t)\text{gm} = \text{gm}V_{RF}\sin(\omega_{RF}t) \quad (11)$$

The mixer actually behaves as a multiplier to sample the RF signal. The RF current multiply LO signal is intermediate-frequency (IF) current. Therefore, we have

$$I_{IF}(t) = I_{RF}(t)V_{LO}(t) \cong (2/\pi)\text{gm}V_{RF}\cos(\omega_{RF} - \omega_{LO})t \quad (12)$$

where Eq. (12) is expanded as a Fourier series. By combining Eq. (12) with another equation, $V_{IF} = I_{IF} \times R_{load}$, the conversion gain can be shown (CG) can be given that

$$Gc = V_{IF}/V_{RF} = (2/\pi)\text{gm1}R_{load} \quad (13)$$

where the transconductance gm1 is $[(2\mu n\ W1\ Id1\ C_{OX})/L1]^{1/2}$, W1 and L1 is the width and length in M1. Id1 is the drain current in M1 and R_{load} is RL1. Therefore, the gain is related to the bias current Id1 and R_{load}.

CIRCUIT IMPLEMENTATION

1. Low noise amplifier

Figure 5 shows a complete schematic of the LNA circuit. Note that in Figure 5, another output buffer stage is added, consisting of transistor M3, R1, R2, and Ld2, for further boosting the LNA gain.

There are two bias circuitries in this LNA: one to bias M1 and M2, and the other to bias M3. Rbias, RB, M4 forms the bias circuitry for transistors M1 and M2. R1 and R2 form another bias circuitry for the output buffer stage transistor M3. The resistor Rbias sets the current for the bias circuitry, which generates the bias voltage at the M1 transistor gate. The RB resistor should be chosen large enough for its equivalent noise to be ignored. This also prevents the input signal from flowing into the bias circuitry. We chose RB at 2 KΩ in this work.

The capacitors Cin, C2, and Cout are the DC

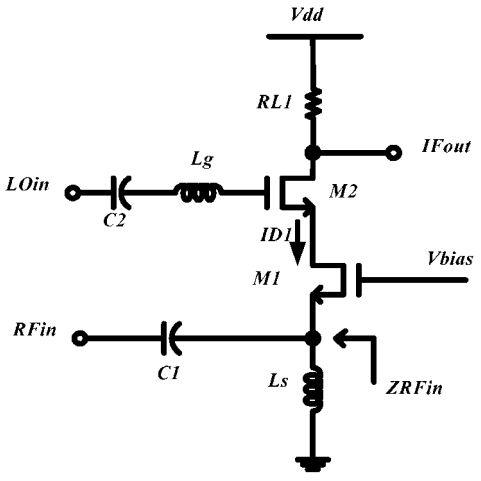

Fig. 4. A single square-law mixer circuit.

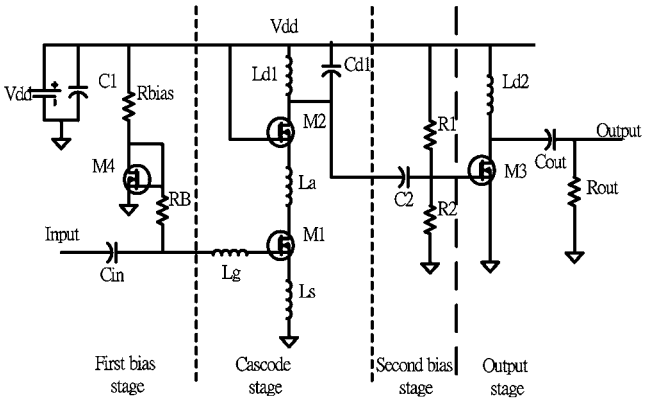

Fig. 5. The complete LNA circuit schematic.

blocking capacitors. Note that C2 is employed to couple the RF signal from the first stage into the output buffer stage, but not the DC signal. The value for C2 must be chosen carefully because it must improve the match between the first stage and the output buffer stage. The overall gain and noise figure will not be optimized with an improper C2 value. The C2 value was chosen as 3 pF in this work. La is the inter-stage matching inductor and its value is 2.56 nH. Lg and Ls were chosen to ensure that input impedance of 50 Ω and resonance at 2.4 GHz were provided. The inductors used in this design were verified inductors. All the inductor values were extracted from the measurement results. The output-matching network consists of Ld2, Cout, and Rout. It is matched to impedance of about 50 Ω.

Because both the input impedance of the common-gate stage and the output impedance of the common-source stage are capacitive, as shown in Figure 5, L_a will cancel the parasitic capacitive loads. In other words, Z_{out} and Z_L can be matched as much as possible by tuning L_a. Because of good power transfer between M1 and M2, the power gain will be increased and the noise will be decreased. L_{d1}, C_{d1} and the terminal capacitance of the other device form a band pass circuit that tunes the LNA to match at 2.4 GHz.

2. Down-conversion mixer

Figure 6 shows the complete Mixer circuit schematic. We added another output buffer stage that consists of the transistors M3, C3 and RL2 to further increase the Mixer gain. There are two bias circuits in this Mixer: one to bias M1, and the other to bias M2. Rg, Rb2, and Mb2 form the bias circuit for transistor M2. Rb1 and Mb1 form another bias circuit for transistor M1. The Rb2 resistor sets the current for the bias circuit, which generates the bias voltage at the gate of transistor M2. The Rg resistor should be chosen large enough for its equivalent noise to be ignored. It also prevents the input signal from flowing into the bias circuit. The capacitors C1, C2 and C3 are the DC blocking capacitors. The R_{load} choice will affect the conversion gain and linearity. This means that R_{L1} cannot be too large; otherwise the output swing will be compressed, especially for low voltage. The output buffer stage of the proposed Mixer consists of M3 and R_{L2}. R_{L2} has the same influence on the conversion gain and linearity. Note that the choice of M2 to make the operating point of M2 must be biased in the saturation region and as close to the triode region as possible. Again, the LO drive must be enough, but not excessive, to promise steady switching. We chose M1 to support the RF input match and isolation from the RF signal port to IF port at 2.4 GHz. The RF port input impedance shows that Z_{RFin} is 1/SC1 + (1/gm1 // SLs). Therefore, C1, Ls and gm1 were chosen to ensure that they provide input impedance of 50 Ω and resonate at 2.4 GHz. The LO port input match consists of Lg and C2. It is matched to an impedance of about 50 Ω.

All of the inductors are implemented on-chip. Figure 7 shows the LNA, mixer and complete receiver layout.

MEASURED RESULTS

This section shows the measured results for the LNA and mixer. The Ansoft Harmonica was used as the RF simulator. Figure 8 shows the measured S parameter for the LNA. The S11 tells us the condition of the input match. The S11 is -20 dB at 2.4 GHz. The power gain is characterized by S21 at 12 dB. The gain is not the maximum at 2.4 GHz. The maximum gain of the LNA is 15 dB at 2 GHz. This is possibly due to an overestimation of the quality factor of the spiral inductors used

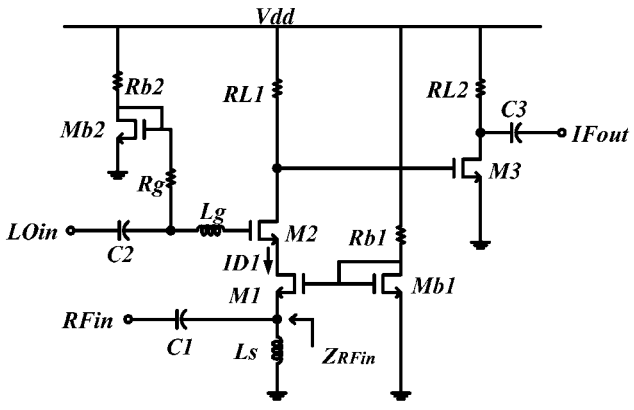

Fig. 6. The complete mixer schematic.

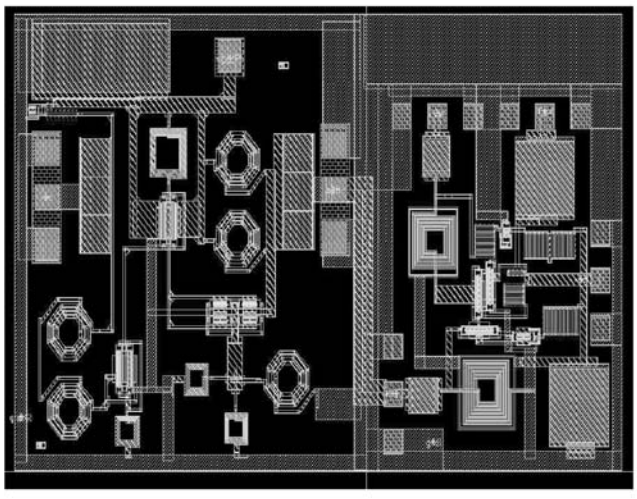

Fig. 7. Layout of the receiver front-end.

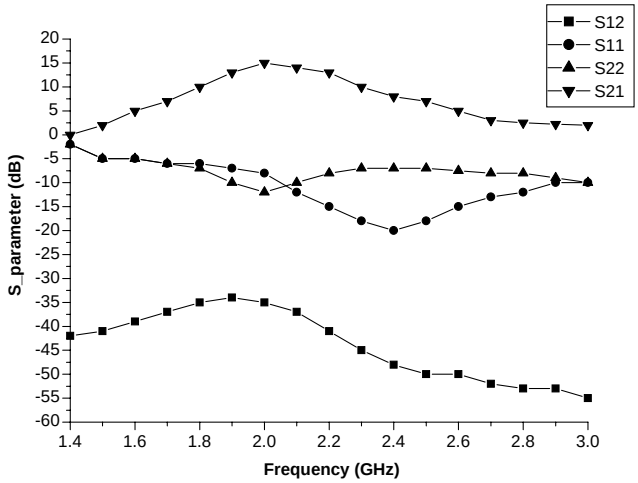

Fig. 8. S parameter of the LNA.

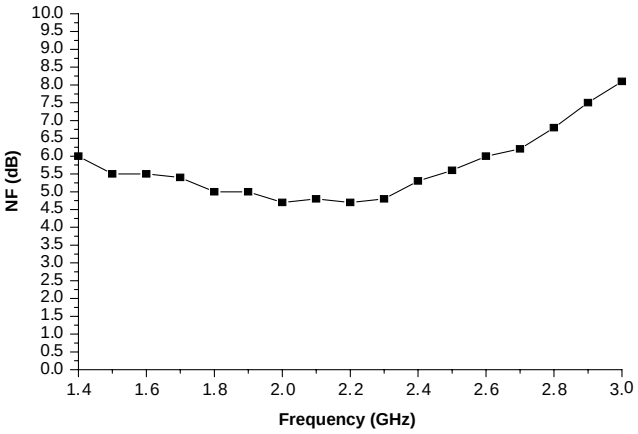

Fig. 9. NF of the LNA.

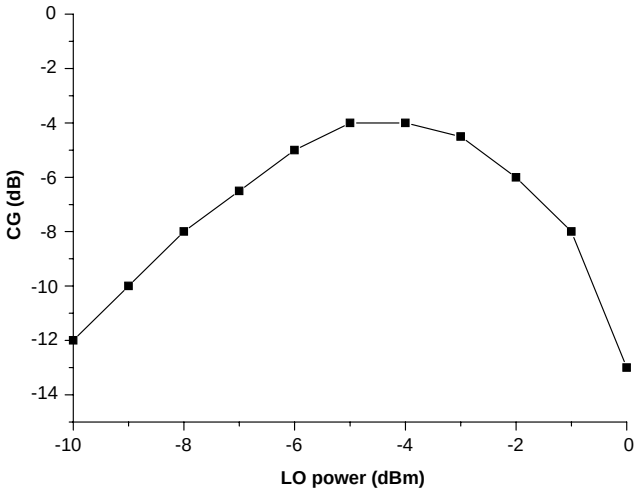

Fig. 10. Mixer conversion gain.

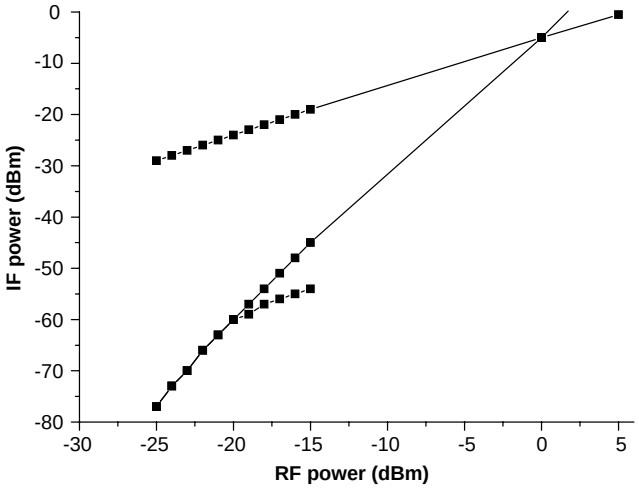

Fig. 11. IIP3 of the mixer.

in the Ld1 load and parasitic capacitance value. The Noise Figure is 4.1 dB at 2 GHz shown in Figure 9. In addition, the mixer was tested using chip-on-board technology. The power conversion gain was -3.5 dB when the LO input power was -3.5 dBm at 2.4 GHz. The conversion gain of mixer is shown in Figure 10. This result is different from the simulation at 2.4 GHz (conversion gain is 1.79 dB). This is possibly due to the parasitics in inductors and capacitors used in the layout. The P-1dB point is -11 dBm and the third-order input intercept point (IIP3) shown in Figure 11 is 0 dBm in the square-law mixer. The port-to-port isolation list follows: LO to IF isolation is 17 dB, RF to IF isolation is 15 dB and LO to RF isolation is 16.8 dB at 2.4 GHz. Table 1 lists the receiver front-end specification. Since this receiver front-end was designed for 1.5 V operation, the optimum measured results were achieved at 1.5 V volt-

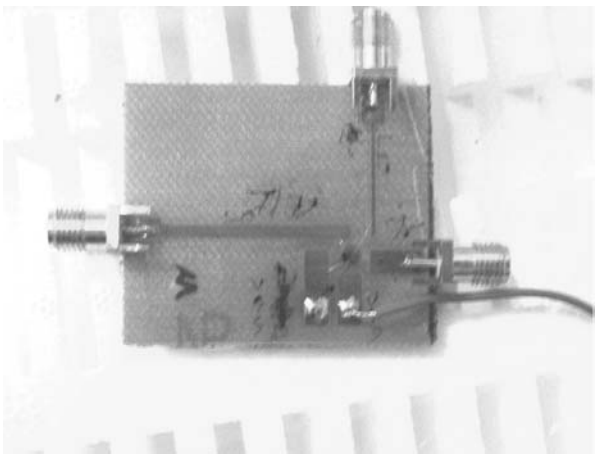

Fig. 12. PCB used in testing the receiver.

Table 1. Measured results for the receiver front-end

Supply voltage	1.5 V	
technology	TSMC 0.35 um CMOS	
RF frequency	2.4 GHz	
IF	100 MHz	
LNA	Voltage gain	12 dB
	Noise figure	4.5 dB
	S11	-20 dB
	S22	-10 dB
	P-1dB	-8 dBm
	Power dissipation	7 mW
Mixer	Conversion gain	-3.5 dB
	LO power	-3.5 dBm
	P-1dB	-11 dBm
	IIP3	0 dBm
	LO-RF isolation	16.8 dB
	LO-IF isolation	17 dB
	RF-IF isolation	15 dB
	Power	2 mW
Receiver	Conversion gain	8.5 dB
	LO power	-3.5 dBm
	P-1dB	-20 dBm
	Power dissipation	9 mW

age supply. The receiver was tested using chip-on-board technology, as shown in Figure 12.

CONCLUSION

The TSMC 0.35 um CMOS high frequency model was used to design a 2.4 GHz receiver front-end. This low noise amplifier provides a gain of 12 dB with a noise figure of 4.5 dB while drawing 7 mW from a 1.5 volt supply. In this study we modified the conventional cascode structure by including an inductor between the common source transistor and the common gate. Taking into consideration the match between the common-gate transistor and the common-source transistor. This will provide system improvement with less power loss along the signal path, low overall noise and high gain in the LNA circuit. A single square-law mixer and common source output buffer was used in this Mixer circuit to check the optimum device size to decrease the total circuit power consumption and provide high linearity performance in an RF mixer circuit.

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