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APPLICATION OF MAXIMUM-EFFICIENCY TRACKING CONTROL TO BACKLIGHT MODULE BASED ON PHASE-LOCKED LOOP TECHNIQUE

Chang-Hua Lin* and Ying Lu**

Key words : CCFL, backlight, PLL, piezoelectric transformer, maximum-efficiency tracking.

ABSTRACT

Maximum-efficiency tracking control applied in the backlight module is proposed in this paper. The backlight system incorporates a phase-locked loop (PLL) as a feedback mechanism to promote both the system efficiency and stability. To overcome the drawbacks of the conventional electromagnetic transformer and to miniaturize the backlight module, the piezoelectric transformer (PT) is adopted for driving the cold cathode fluorescent lamp (CCFL). To avoid the system efficiency decreases due to the temperature effect of PT, the PLL is utilized to track immediately the optimal operating frequency of PT for achieving maximum output efficiency under various ambient temperatures. The feedback parameter used in the presented system is the phase component instead of the traditionally employed lamp current amplitude. A simple model and the design procedures are both constructed by reasonable parameter simplification and combination schemes. Complete analysis and design considerations are discussed in detail in this paper. Experimental results agree with the theoretical prediction.

I. INTRODUCTION

The demands for thin and flat display panels are increasing drastically, due to the popularity of information apparatus, to replace conventional CRT displays used in many products with different panel sizes. The backlight module is a crucial component for driving light source in flat display panel (FDP) technologies, and its performance will influence the display quality of FDP. The LCD combined with Cold Cathode Fluorescent Lamp (CCFL) satisfies the increasing need on display performance, size, and efficiency [4]. In the past, the conventional electromagnetic transformers were generally adopted in the backlight module design to boost output voltage for driving CCFL. However, the conventional transformer will cause the magnetic hysteresis loss and electromagnetic interference and thus decrease the efficiency of energy conversion. In 1956, Rosen presented the direct and converse piezoelectric effect of piezoelectric components as the mechanism of mechanical and electrical energy interchange, which provides high conversion efficiency by transferring electrical energy via the polarized and mechanical vibration medium. Since piezoelectric transformer (PT) can sustain its inherent high voltage gain while matching high impedance load with optimal efficiency, it is applicable to driving high-voltage high-impedance lamps, such as CCFL.

In addition, PT possesses many advantages, namely, compact size, high efficiency, low power losses and free of EMI. Moreover, PT not only can provide high voltage gain but also is easy to realize the miniature design of FDP, in which the backlight module is joined with PT [5], [7], [10]. However, the materials which have higher values of electromechanical coupling coefficient generally hold poorer temperature stabilities. Due to the susceptibility of PT to the environmental temperature, the system efficiency and stability are easy to be adversely affected. Moreover, because of the narrow bandwidth characteristics, the transient response of PT is much slower with the traditional voltage-controlled oscillator (VCO) feedback mechanism. Additionally, an excess of operating frequency deviation can lead to the reduction of conversion efficiency [6]. Hence, this paper proposes a novel control scheme to deal with the above-mentioned problems. Table I compares the proposed backlight inverter with the conventional one in aspects such as EMI, control mechanism, efficiency, and etc. [3, 4, 5, 8, 10]. The presented control scheme exploits the phase-locked loop (PLL) to fast track the optimal operating frequency of PT based on the variation of its loads or environmental temperature. The captured phase component rather than the traditionally used lamp current amplitude is utilized as the feedback parameter to obtain the maximum output gain, and then to achieve the maximum output efficiency by fixing the phase difference between the input voltage and the output current. Furthermore, the lock-in range of PLL can be set to the operating bandwidth

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Table 1. Comparisons between the proposed backlight inverter and conventional one.

Item	Conventional inverter	Proposed inverter
Boost transformer	Electromagnetic transformer	Piezoelectric transformer
EMI	High	Low
Suitable for thin profile	No	Yes
Operating bandwidth	Wide	Narrow
Feedback parameter	Lamp current	Phase difference
Control mechanism	VCO	PLL
Temperature effect	Immune	Susceptible
efficiency	Low	Maintain maximum-efficiency

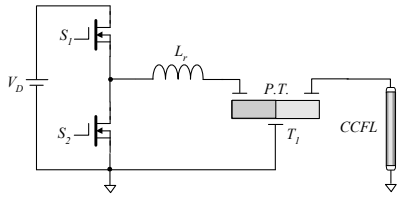

Fig. 1. Half-bridge resonant inverter with piezoelectric transformer.

of piezoelectric transformer during normal operation state. As the resonant characteristics of PT is influenced by the environmental temperature, the PLL will rapidly track the optimum operating frequency within the lock-in range, and maintain the synchronization state so as to achieve the maximum-efficiency tracking, and thus also eliminate the temperature effect of PT.

II. ANALYSIS OF HALF-BRIDGE RESONANT INVERTER

Fig. 1 shows the employed half-bridge resonant inverter, which consists of a resonant inductor L_r, a piezoelectric transformer T_1, and two alternative switching power switches S_1, S_2. When the operating frequency of the circuit is close to the resonant frequency of the employed inverter, the harmonics and DC component of the current flowing in the circuit will be filtered out due to the high quality factor (Q_L) of the main circuit [3], [8]. Therefore, sinusoidal voltage and current can be produced to start and drive CCFL. Fig. 2a illustrates the equivalent main circuit of Fig. 1 in steady state, in which a PT equivalent model, an external resonant inductor L_r, and a secondary reflected impedance are included to form a resonant tank [4], [6]. The secondary reflected impedance comprises lamp impedance R_ℓ and parasitic capacitance.

The mathematical models of derived circuits presented in [8], [10] are too complicated due to numerous internal equivalent parameters of PT. Therefore, reasonable parameter simplification and combination schemes are utilized to decide the desired parameters of circuit components and to derive a simple

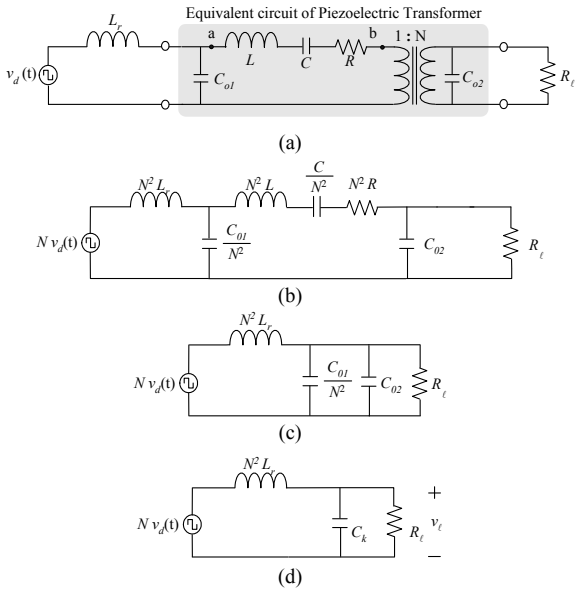

Fig. 2. (a) Equivalent circuit model of resonant inverter with PT, (b) equivalent circuit of 2a, (c) simplified circuit of 2b, (d) simplified circuit of 2c.

mathematical model. To simplify the circuit model, the parasitic capacitance is neglected and the CCFL is replaced by R_ℓ. The primary components of PT are converted equivalently to the secondary ones of PT and the resultant circuit is shown in Fig. 2b. When PT is operating in its resonant frequency, R, L, and C elements in the circuit model are considered as short-circuited due to the voltages of inductor L and capacitor C having the same magnitudes but opposite polarities. Thus, we can further simplify the circuit to be equivalent to a resonant circuit structure as shown in Fig. 2c. Fig. 2d illustrates the final reduction circuit model, where

$$C_k = \frac{C_{01}}{N^2} + C_{02} \tag{1}$$

In general, CCFL should be started with high voltage in normal situation; however, the backlight module is usually supplied with low voltage. Therefore, equation (2) is used to determine the relationship between the steady-state operating voltage and the input dc voltage V_D

$$\left|\frac{v_\ell(j\omega)}{v_d(j\omega)}\right| = \frac{\sqrt{2}v_{\ell,rms}}{\frac{4}{\pi}\frac{V_D}{2}} \tag{2}$$

The transfer function of input voltage v_d(t) to lamp voltage v_ℓ can be calculated from Fig. 2d. If the sinusoidal approximation method is employed, the transfer function is obtained as follows

$$\frac{v_\ell(j\omega)}{v_d(j\omega)} = \frac{NR_\ell}{(R_\ell - \omega^2 N^2 L_r C_k R_\ell) + j\omega(N^2 L_r)} \tag{3}$$

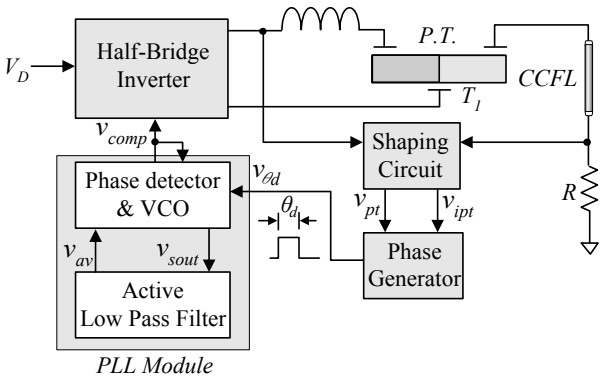

Fig. 3. The block diagram of the single-stage backlight module based on phase-locked loop technique.

The magnitude and phase angle of (3) are respectively expressed as

$$\left|\frac{v_\ell(j\omega)}{v_d(j\omega)}\right| = \frac{NR_\ell}{\sqrt{(R_\ell - \omega^2 N^2 L_r C_k R_\ell)^2 + (\omega N^2 L_r)^2}} \tag{4}$$

$$\theta_d = -\tan^{-1}\frac{\omega N^2 L_r}{R_\ell - \omega^2 N^2 L_r C_k R_\ell} \tag{5}$$

From (4) and (5), we see that the lamp voltage is related to the input voltage, the operating frequency, lamp characteristics, transformer characteristics (turns ratio N) and the resonant tank components (including resonant inductor L_r and equivalent resonant capacitor C_k).

III. CONTROL SCHEME FOR TRACKING THE OPTIMAL OPERATING FREQUENCY

The electric characteristics of PT are highly sensitive to the variation of environmental parameters such as load variation and environmental temperature change, which will result in the resonant frequency variation and thus significantly influence the system efficiency [9]. Hence, this paper presents a controller based on the PLL technique to simultaneously get the phases of input voltage and secondary output current of PT for tracking the optimal operating frequency of PT so as to achieve the maximum output gain and then to retain the maximum output efficiency by fixing the phase difference between said input voltage and said output current. The basic structure of PLL is composed of a phase detector, a low pass filter, and a voltage-controlled oscillator (VCO) [7]. Fig. 3 shows the block diagram of complete system configuration. The shaping and phase generator circuit senses the phase difference θ_d between the input voltage v_{pt} and the secondary output current signal v_{ipt}. If θ_d changes, the active low pass filter will generate an average voltage v_{av} corresponding to the output of phase detector to regulate VCO and thus synchronize the output frequency of PLL.

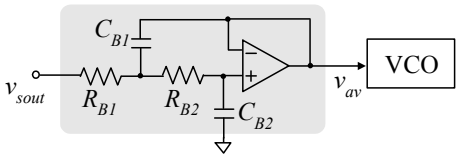

Fig. 4. The circuit configuration of the adopted active low pass filter.

In Fig. 3, the phase detector is applied respectively with the output signal v_{comp} of VCO and the external signal $v_{\theta d}$ for detecting their frequency variation and the phase difference between these two input signals. When the frequencies or phases of v_{comp} and $v_{\theta d}$ are different, the phase detector will generate an output signal v_{sout} indicating the variation amount of frequency or phase, to immediately adjust the output frequency of VCO, and in turn regulate the operating frequency of the inverter such that the phases of v_{comp} and $v_{\theta d}$ can be shifted back to their original lock-in states. Hence, the input voltage and the secondary output current of PT maintain their synchronization with fixed phase difference to accomplish the tracking of the maximum efficiency. In addition, with the capture range setting of PLL, PT can be operated under the preset central frequency f_o (i.e., resonant frequency) [2] during the initial starting period in the condition of absence of the feedback signal comparison so that CCFL is started smoothly. Moreover, the lock-in range of PLL can be set to the operating bandwidth of PT during normal operation state. When the resonant characteristics of PT is influenced by the environmental temperature, the PLL will rapidly track the optimum operating frequency within the lock-in range, and maintain the synchronization between v_{pt} and v_{ipt} so as to achieve the maximum-efficiency tracking, and thus also eliminate the temperature effect of PT. The frequency deviation Δf_L of PLL can be determined according to the specification of PT. Hence, the minimum operating frequency $f_{\min}$ and the maximum operating frequency $f_{\max}$ can be derived respectively as follows:

$$f_{\min} = f_o - \Delta f_L \tag{6}$$

$$f_{\max} = f_o + \Delta f_L \tag{7}$$

From (6) and (7), parameter α is defined as

$$\alpha = \frac{f_{\max}}{f_{\min}} \tag{8}$$

Then we can use α and characteristic curves of CD4046BC [2] to estimate the value of PLL's timing components, R_1 and R_2.

In PLL design, the stability of VCO is mainly affected by the design of phase detector and low pass filter. This paper presents an active second-order low pass filter, having the advantages of more rectangular frequency response and better noise suppression, to cope with the aforementioned drawback. Fig. 4 describes the realization circuit of the adopted active

filter. The active filter receives the input signal v_{sout} from the output of phase detector, filters out its high frequency components, and then generates a corresponding dc voltage v_{av} to modulate VCO. For simplifying the circuit design, we assume that

$$R_{B1} = R_{B2} = R_B \tag{9}$$

The transfer function of active filter is expressed below

$$\frac{v_{av}(s)}{v_{sout}(s)} = \frac{\dfrac{1}{R_B{}^2 C_{B1} C_{B2}}}{s^2 + \dfrac{2}{R_B C_{B1}} s + \dfrac{1}{R_B{}^2 C_{B1} C_{B2}}} = \frac{\omega_n{}^2}{s^2 + 2\zeta\omega_n s + \omega_n{}^2} \tag{10}$$

where

$$\omega_n = \frac{1}{R\sqrt{C_{B1} C_{B2}}} \tag{11}$$

$$\zeta\omega_n = \frac{1}{RC_{B1}} \tag{12}$$

Substituting (11) into (12) yields

$$\varsigma = \sqrt{\frac{C_{B2}}{C_{B1}}} \tag{13}$$

IV. DESIGN CONSIDERATIONS

The PT utilized in the paper is EFTU14R0M02, which has rated power of 4W, resonant frequency of 54.2±1kHz, input voltage of $22V_{rms(max)}$, input current of $500mA_{rms(max)}$, output voltage of $820V_{rms(max)}$, output current of $7mA_{rms(max)}$, and operating temperature range of -10℃~60℃.The CCFL used is FL-30266AE, which has rated power of 3.4W, operating voltage v_ℓ of $620V_{rms}$, operating current i_ℓ of 5±1mA, and starting voltage v_{start} of $930V_{rms}$. The operating frequency of CCFL is generally within the range of 20~80kHz. In this paper, we select the operating frequency f_o of 54.2kHz and input voltage $V_D = 12V_{DC}$. The most important parameters in the proposed circuit structure are the external resonant inductor L_r and resonant capacitor C_k of PT, as well as R_{B1}, R_{B2}, C_{B1}, and C_{B2} of active filter. The considerations and steps to determine these parameters design are discussed below.

1. Measuring the parameters of the equivalent PT model

Fig. 2a shows the equivalent circuit model of PT operating in its resonant frequency. The parameters of the employed PT are measured with an impedance analyzer HP-4194A. The related parameter values measured are shown below.

C_{01} = 99.66nF	C = 6.21nF	R = 1.26Ω
C_{02} = 9.09pF	L = 1.22mH	N = 55

2. Selecting the proper value of resonant inductor Lr

The half-bridge parallel-resonant inverter is incorporated with PT, such that the external resonant inductor L_r and equivalent internal input capacitor C_{01} can filter out high order harmonic components of voltage and current and generate the sinusoidal ones for the ideal transformer shown in Fig. 2a. The selection of the value of resonant inductor L_r is crucial to the stability of the whole resonant circuit. In steady state, we can substitute the rated lamp voltage and input dc voltage into (2) to obtain the following equation

$$\left|\frac{v_\ell(j\omega)}{v_d(j\omega)}\right| = 620\sqrt{2}/(4/\pi \times 12/2) = 115 \tag{14}$$

Substituting the measured parameters of PT, lamp impedance $R_\ell = v_\ell / i_\ell$=111.82kΩ, operating frequency f_o =54.2kHz and (14) into (4) yields resonant inductor L_r =35.3μH (use 36μH).

3) Estimating the operating frequency range of PLL

The PLL's timing components, R_1, R_2, and C_1 can be chosen to set the lock-in range [1]. The central frequency f_o of PLL is preset to the operating frequency f_o=54.2kHz. The frequency deviation Δf_L of ±1kHz is substituted into (6) to yield the minimum operating frequency f_{min} of PLL shown below

$$f_{\min} = f_o - \Delta f_L = 53.2kHz \tag{15}$$

Using the characteristic curve of PLL module [1] with the frequency of (15) estimates R_2=10kΩ and C_1=2nF (use 2.2nF). From (7), the maximum operating frequency of PLL f_{max}=55.2kHz is obtained. Then substituting the minimum and maximum operating frequencies into (8) yields α as follows:

$$\alpha = \frac{55.2kHz}{53.2kHz} \cong 1.04 \tag{16}$$

Using the characteristic curve of PLL module with α of (16) estimates

$$\frac{R_2}{R_1} = 0.25 \tag{17}$$

Entering (17) into [1] finds $R_1 \cong 30k\Omega$ (use 30.1kΩ).

4) Determining parameters of active low pass filter

With the given voltage-to-frequency conversion gain of VCO as 6kHz/V and the lock-in range of PLL as f_o±1kHz, the percent maximum overshoot of unit-step response acquired is about 20%.From (18), we can obtain the damping ratio ζ=0.46.

$$\%OS = \exp[-\frac{\zeta\pi}{\sqrt{1-\zeta^2}}]\times 100 \tag{18}$$

Because the capture range of PLL is approximate to the cut off frequency of active filter in the proposed configuration, we can define the error tolerance of final value in unit-step response within 2%, as indicated in the following inequality

$$e^{-\zeta\omega_n T_s} \le 0.02 \tag{19}$$

where T_s is the settling time. Due to persistence of vision, the

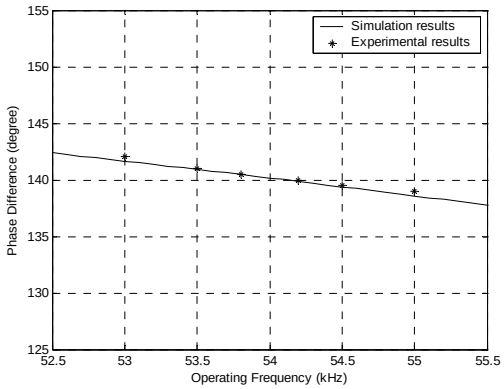

Fig. 5. Simulation and experimental results of phase difference versus operating frequency.

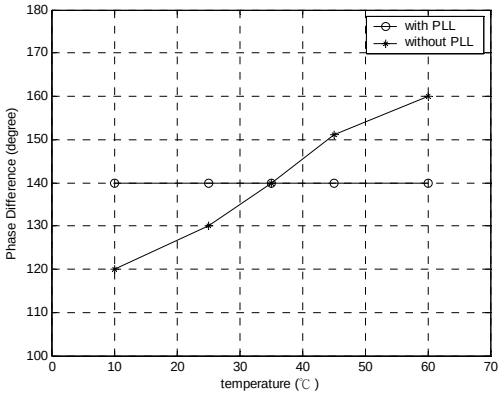

Fig. 6. Experimental results of phase difference versus temperatures with and without PLL.

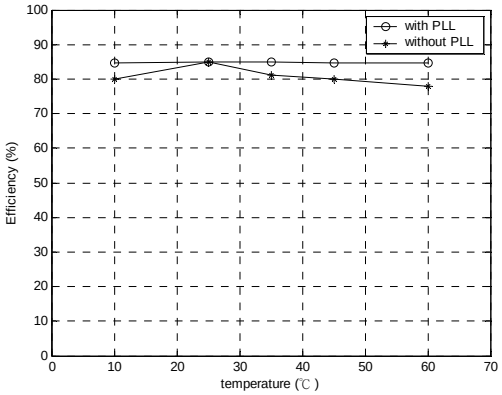

Fig. 7. System efficiency versus temperatures with and without PLL.

settling time T_s is set to 10ms to avoid the lamp flickering interval. Substituting T_s and ζ into (19) acquires the cut off frequency of active filter ω_n=850.44rad/s. Then, substituting ζ, ω_n, and C_{B1}=22nF into (11)-(13), the required data of R_{B1}=R_{B2}=116kΩ (use 120kΩ) and C_{B2}=4.65nF (use 4.7nF) of the active filter are obtained. By applying R_{B1}=R_{B2}=120kΩ, C_{B1}=22nF, and C_{B2}=4.7nF to the active filter, we can get the desired filter characteristics for the employed PLL mechanism.

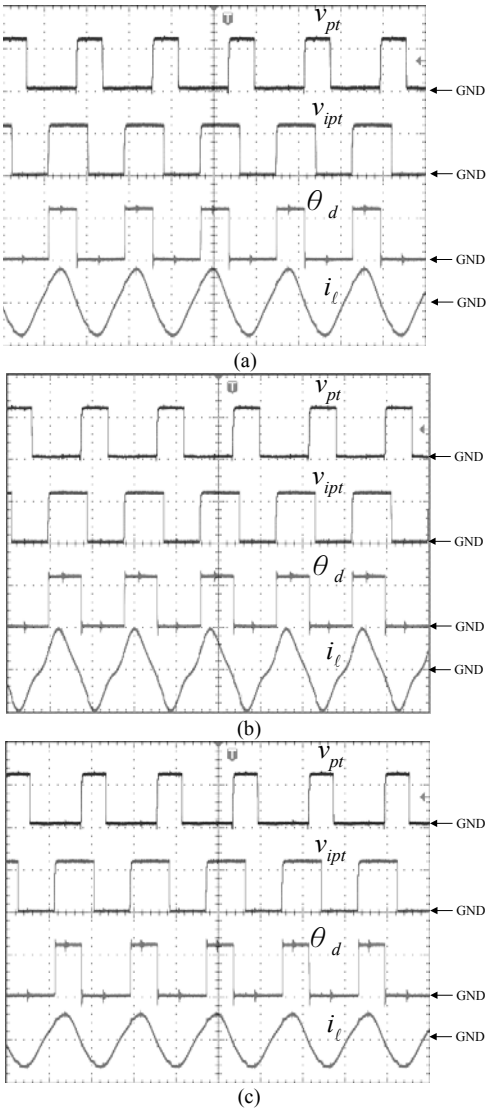

Fig. 8. Measured waveforms of v_{pt}, v_{ipt}, θ_d and i_ℓ without PLL under various environmental temperatures (a) 27.5℃ (b) 60℃ (c) 10℃ (Ver: 10V/div for v_{pt}; Ver: 10V/div for v_{ipt}; Ver: 10V/div for θ_d; Ver: 10mA/div for i_ℓ; Hor: 10μs/div).

V. SIMULATIONS AND EXPERIMENTAL RESULTS

The phase differences associated with various operating frequencies, obtained from the experimentation as well as simulation based on (5), are plotted in Fig. 5, which demonstrates the close agreement between the experimental results and the theoretical prediction. Figs. 6 and 7 display the phase difference and system efficiency, respectively, under various temperatures with and without PLL mechanism. Because the PT is vulnerable to the variation of environmental temperature and the resonant characteristics are affected accordingly, therefore, without the assistance of the PLL, both the phase difference and the system efficiency are altered with the ambient temperature. Fig. 8a~8c demonstrate the measured waveforms of input voltage v_{pt} and secondary output current

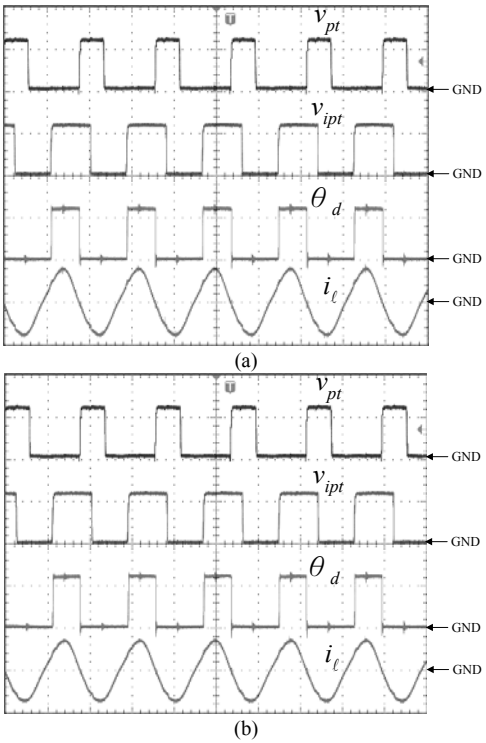

Fig. 9. **Measured waveforms of v_{pt}, v_{ipt}, θ_d and i_ℓ with PLL mechanism under various environmental temperatures (a) 60℃ (b) 10℃ (Ver: 10V/div for v_{pt}; Ver: 10V/div for v_{ipt}; Ver: 10V/div for θ_d; Ver: 10mA/div for i_ℓ; Hor: 10μs/div).**

signal v_{ipt} of PT, phase difference θ_d acquired by phase detector, and lamp current i_ℓ under different environmental temperatures, respectively, without PLL.

Fig. 8a shows the measured waveforms in room temperature of 27.5℃. As the lagging phase difference θ_d of input voltage v_{pt} to secondary output current v_{ipt} is about 140° and lamp current i_ℓ is 5.5mA$_{rms}$. At this operating temperature, the employed PT can provide high conversion characteristic and the CCFL operates at the rated power of 3.4W. It is observed that the input voltage is 12V, while the input current is approximately 0.334A, and, hence, the input power is about 4.009W. The system efficiency η can be calculated from the lamp power divided by the input power, resulting in the maximum-efficiency of 84.8%. When PT operates under the environmental temperature near 60℃, as shown in FIG. 8B, the phase difference θ_d increases to 160°, lamp current i_ℓ escalates to 7.1mA$_{rms}$, and system efficiency degrades to 78 %. As PT operates under the environmental temperature about 10℃, as illustrated in Fig. 8c, the phase difference θ_d decreases to 120°, lamp current i_ℓ reduces to 4.5 mA$_{rms}$, and system efficiency cuts back to 80%. From the experimental results, we can observe that PT is sensitive to the environmental temperature in open-loop conFiguration. Therefore, a feedback mechanism is essential to maintain maximum-efficiency under various environment temperatures.

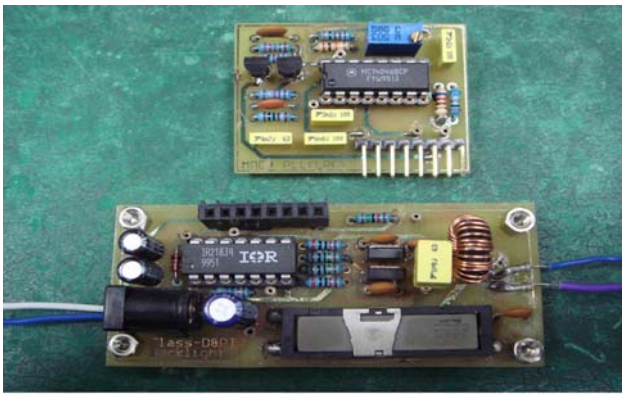

Fig. 10. **The prototype of the proposed backlight system (upper: controller; lower: resonant inverter).**

To verify the validity of the proposed control strategy, the employed system incorporated with a PLL circuit forming the closed-loop configuration is measured. Fig. 9a~9b present the measured waveforms under the environmental temperatures of 60℃ and 10℃, respectively. It is noted that the measured phase difference θ_d and lamp current i_ℓ of these two conditions are the same as those in room temperature condition, that is, θ_d = 140° and i_ℓ = 5.5mA$_{rms}$, the deviations of frequency each are within 1kHz so that the system operates in a stable state, and the overall efficiencies each are above 84%. Therefore, the proposed control strategy not only provides the capability to eliminate the temperature effect of PT by locking the constant phase difference between the primary input voltage and the secondary output current of PT with PLL, but also offers a steady output current from PT to drive CCFL and hence effectively extend the lamp life. The prototype of the proposed backlight system is illustrated in Fig. 10.

VI. CONCLUSION

First, a half-bridge resonant inverter is incorporated with a piezoelectric transformer to drive the cold-cathode fluorescent lamp. Then, the PLL technique is adopted to track the optimal operating frequency of PT by locking the constant phase difference between the primary input voltage and the secondary output current of PT, so as to eliminate the temperature effect and thus enhance the system stability. Finally, an active low pass filter is employed in the PLL to improve the frequency response characteristics of the filter and suppress the noise, such that the system stability can be promoted substantially. The system efficiencies are promoted above 85% in all test conditions.

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