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DESIGN AND IMPLEMENTATION OF DSTATCOM FOR FAST LOAD COMPENSATION OF UNBALANCED LOADS

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Key words: DSTATCOM, hardware implementation, load compensation, symmetrical components.

ABSTRACT

This paper proposes a distribution level static synchronous compensator (DSTATCOM) for fast load compensation of unbalanced loads in electric power distribution systems. For fast response requirement, a new feedforward compensation scheme is derived and employed in the paper. First, the compensation scheme of the DSTATCOM is derived with the symmetrical components method. Then, computer simulation with the program Matlab/Simulink preliminarily verifies the effectiveness of the proposed DSTATCOM. Accordingly, a hardware prototype is built with a floating-point DSP TMS320C6711-based system. Use of a current-regulated PWM (CRPWM) inverter as the power stage of the DSTATCOM generates needed compensation currents for real-time load compensation. Finally, experimental results confirm the effectiveness of the proposed DSTATCOM.

I. INTRODUCTION

Electric power quality (EPQ) problems mainly include unbalance voltage and current, flicker, harmonics, voltage sag, dip, swell, and power interruption [4]. These power quality problems may cause abnormal operations of facilities or even trip protection devices. Hence, the maintenance and improvement of electric power quality have become an important scenario today.

The term "load compensation" means to balance unbalanced load and correct load power factor to unity at the same time. Load compensation is very important for many applications such as compensations of single-phase railway systems and electric arc furnace systems. Since 1970, static var compensators (SVCs) have widely been used in electric power industry for power quality improvements. With phase-independent operation ability, SVCs can effectively compensate flicker, unbalanced load, and correct load power factor [3, 7].

However, the thyristor-controlled reactor (TCR) of the SVC has significant space demand. Furthermore, due to the natural communication limit of the thyristors used in the TCR, SVC cannot respond immediately with the change of load. This leads to five ms to a half-cycle of time delay. Hence, SVC has merely a maximum compensation ability of 65% to flicker [8]. The response time and compensation ability of SVCs still need improvements. Distribution level static synchronous compensator (DSTATCOM) [2, 5, 9, 10, 11, 12, 15, 16], which is one of the FACTS elements [6, 13, 14], is a newly developed compensator in electric power industry. Compared to existing SVCs, DSTATCOM has quicker response time and compact structure. It is expected that DSTATCOM will replace the roles of SVCs in the near future.

This paper proposes a DSTATCOM for real-time load compensation of three-phase three-wire power distribution systems with unbalanced loads. First, a new feedforward compensation scheme is developed for the DSTATCOM with the symmetrical components method for fast response requirement. In this way, the DSTATCOM can quickly balance the unbalanced load and correct the power factor at the same time. Then, the system is built and simulated with the program Matlab/Simulink. Accordingly, a hardware prototype is built by using a floating-point DSP TMS320C6711-based system. Finally, experimental results are given for verification.

II. COMPENSATION SCHEME OF DSTATCOM

Figure 1 shows a radial type electric power distribution system feeding an unbalanced load. A DSTACOM is installed in parallel with the unbalance load for on-site load compensation. The reactive power output of the DSTATCOM in each phase, which is inductive or capacitive, can be independently controlled by the controller of the DSTATCOM for real-time load compensation. The method of symmetrical components is used in the paper for deriving the compensation scheme of the DSTATCOM. First in Fig. 1, the line-to-line load bus voltages are transferred to positive- and negative-sequence components by using the symmetrical components transformation matrix [T], as defined in (1). The three-phase unbal-

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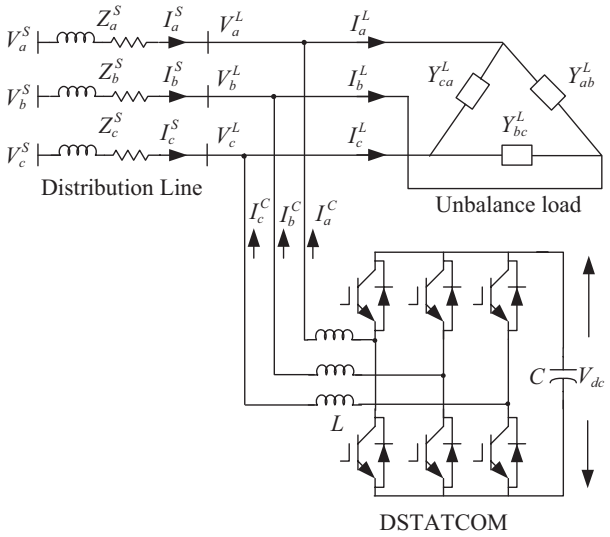

Fig. 1. A radial distribution system with an unbalance load and a DSTATCOM.

anced load currents in the *a-b-c* reference frame can be expressed as (2).

$$\begin{bmatrix} \bar{V}_{ab}^{L} \\ \bar{V}_{bc}^{L} \\ \bar{V}_{ca}^{L} \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & \alpha^2 & \alpha \\ 1 & \alpha & \alpha^2 \end{bmatrix} \begin{bmatrix} \bar{V}_{ll,0}^{L} \\ \bar{V}_{ll,1}^{L} \\ \bar{V}_{ll,2}^{L} \end{bmatrix} = [T] \begin{bmatrix} \bar{V}_{ll,0}^{L} \\ \bar{V}_{ll,1}^{L} \\ \bar{V}_{ll,2}^{L} \end{bmatrix}, \ \alpha = e^{j(2/3)\pi} \quad (1)$$

$$\begin{bmatrix} \bar{I}_{a}^{L} \\ \bar{I}_{b}^{L} \\ \bar{I}_{c}^{L} \end{bmatrix} = \begin{bmatrix} Y_{ab}^{L} & 0 & -Y_{ca}^{L} \\ -Y_{ab}^{L} & Y_{bc}^{L} & 0 \\ 0 & -Y_{bc}^{L} & Y_{ca}^{L} \end{bmatrix} \begin{bmatrix} \bar{V}_{ab}^{L} \\ \bar{V}_{bc}^{L} \\ \bar{V}_{ca}^{L} \end{bmatrix} \quad (2)$$

Applying the symmetrical components method transfers the three-phase load currents to positive- and negative-sequence components, as shown in (3) and (4). In (3) and (4), the line-to-line voltages are assumed equal to simplify the derivation of the compensation scheme.

$$\bar{I}_{1}^{L} = (1-\alpha) Y_{0}^{L} V_{ll}^{L} \quad (3)$$

$$\bar{I}_{2}^{L} = (1-\alpha^2) Y_{1}^{L} V_{ll}^{L} \quad (4)$$

$$\text{Where: } \begin{bmatrix} Y_{0}^{L} \\ Y_{1}^{L} \\ Y_{2}^{L} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & \alpha & \alpha^2 \\ 1 & \alpha^2 & \alpha \end{bmatrix} \begin{bmatrix} Y_{ab}^{L} \\ Y_{bc}^{L} \\ Y_{ca}^{L} \end{bmatrix}, \ V_{ll}^{L} = \left| \bar{V}_{ll,1}^{L} \right|$$

The detection of the load power can be obtained via two-wattmeter method, as shown in (5)~(6). From (5)~(6), the positive- and negative-sequence load currents are represented with line-to-line active and reactive powers, as shown in (7).

$$\left(\bar{V}_{ab}^{L}\right)^{*} (\bar{I}_{a}^{L}) = (V_{ll}^{L} \angle -30°)[(\bar{I}_{1}^{L}) + (\bar{I}_{2}^{L})] \quad (5)$$

$$\left(\bar{V}_{cb}^{L}\right)^{*} (\bar{I}_{c}^{L}) = (V_{ll}^{L} \angle -90°)[\alpha(\bar{I}_{1}^{L}) + \alpha^2 (\bar{I}_{2}^{L})] \quad (6)$$

$$\begin{bmatrix} \bar{I}_{1}^{L} \\ \bar{I}_{2}^{L} \end{bmatrix} = \frac{1}{\left|V_{ll}^{L}\right|(\alpha-1)} \begin{bmatrix} 1\angle 150° & 1\angle 150° \\ 1\angle -150° & 1\angle -30° \end{bmatrix} \begin{bmatrix} P_{ab}^{L} - jQ_{ab}^{L} \\ P_{cb}^{L} - jQ_{cb}^{L} \end{bmatrix} \quad (7)$$

For fast load compensation, the DSTATCOM should compensate the imaginary part of the positive-sequence load current and the entire negative-sequence load current in (7) as soon as possible. In this way, the power source supplies only real part of the positive-sequence load current. Since no zero-sequence component appears in three-phase three-wire system, the compensation current can be derived from (8)~(10). Finally, the needed compensation current of the DSTATCOM for load compensation is obtained, as shown in (11).

$$\bar{I}_{a}^{C} = \mathrm{Im}(\bar{I}_{1}^{L}) + \bar{I}_{2}^{L} \quad (8)$$

$$\bar{I}_{b}^{C} = \alpha^2 \,\mathrm{Im}(\bar{I}_{1}^{L}) + \alpha \bar{I}_{2}^{L} \quad (9)$$

$$\bar{I}_{c}^{C} = \alpha \,\mathrm{Im}(\bar{I}_{1}^{L}) + \alpha^2 \bar{I}_{2}^{L} \quad (10)$$

$$\begin{bmatrix} \bar{I}_{a}^{C} \\ \bar{I}_{b}^{C} \\ \bar{I}_{c}^{C} \end{bmatrix} = \begin{bmatrix} \frac{1}{2\sqrt{3}} + j\frac{1}{2} & \frac{-1}{\sqrt{3}} & \frac{1}{2} - j\frac{\sqrt{3}}{2} & 0 \\ -\frac{1}{\sqrt{3}} & \frac{1}{2\sqrt{3}} - j\frac{1}{2} & \frac{-1}{2} + j\frac{\sqrt{3}}{2} & -1 \\ \frac{1}{2\sqrt{3}} - j\frac{1}{2} & \frac{1}{2\sqrt{3}} + j\frac{1}{2} & 0 & 1 \end{bmatrix} \begin{bmatrix} P_{ab}^{L}/V_{ll}^{L} \\ P_{cb}^{L}/V_{ll}^{L} \\ Q_{ab}^{L}/V_{ll}^{L} \\ Q_{cb}^{L}/V_{ll}^{L} \end{bmatrix} \quad (11)$$

According to (11), the DSTATCOM is now treated as a current-controlled source to locally supply the needed compensation current for on-site load compensation. In the implementation, a current-regulated PWM (CRPWM) inverter is used as the power stage of the DSTATCOM for generating the compensation current, as shown in Fig. 1. In order to keep the dc-link voltage of the inverter in the DSTATCOM at an assigned level during operation, the DSTATCOM needs to absorb active power from the power source to supply the power losses and charge the dc-link capacitor in the DSTATCOM. Hence, use of a P-I type feedback controller in the DSTATCOM controller regulates the active current $|I_r|$ of the DSTATCOM,

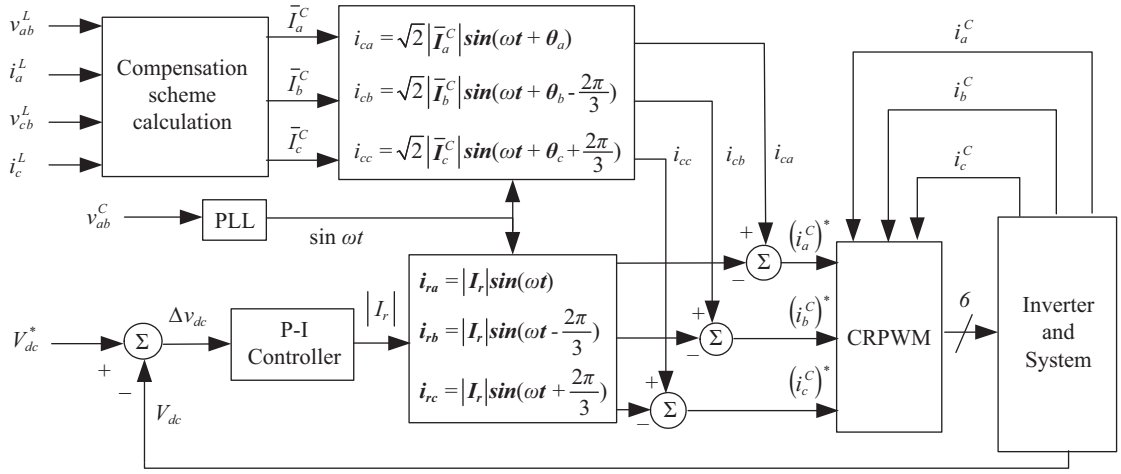

Fig. 2. Block diagram of the proposed DSTATCOM controller.

as shown in (12). The overall compensation scheme of the DSTATCOM is now completed.

$$|I_r| = K_p \Delta v_{dc} + K_i \int \Delta v_{dc} dt \tag{12}$$

For fast real-time compensation, the DSTATCOM needs to detect the line-to-line power data very quickly to calculate the needed compensation current, as shown in (8). The needed line-to-line power data are P_{ab}^L, Q_{ab}^L, P_{cb}^L, Q_{cb}^L, V_{ll}^L. A fast detection method for these power data is described in [1]. Moreover, the three-phase power data measurements can also be incorporated in the controller of the DSTATCOM. With a high performance DSP-based system, the compensation scheme and other necessary functions regarding power detections can be implemented very easily. In this way, the necessity for measuring instruments is reduced. This significantly reduces the constructing cost of the DSTATCOM and enhances the system reliability.

Figure 2 shows the block diagram of the proposed DSTATCOM controller for the DSTATCOM. According to (11), the DSTATCOM controller calculates the compensation current commands $\bar{I}_a^C$, $\bar{I}_b^C$, $\bar{I}_c^C$ by using line-to-line voltages v_{ab}^L, v_{cb}^L and line currents i_a^L, i_c^L. The instantaneous compensation currents are obtained with the aid of the synchronous signal sin ωt via a PLL circuit. Additionally, the dc-link voltage is maintained by supplying a real part of compensation current $|I_r|$ via a P-I controller, as shown in (12). With the same synchronous signal sin ωt, the instantaneous current for active power balance is also yielded. Combining the above two currents generates the needed three-phase current command signals $\left(i_a^C\right)^*$, $\left(i_b^C\right)^*$, $\left(i_c^C\right)^*$ for the DSTATCOM.

The paper employees a current-regulated PWM (CRPWM) inverter as the power stage of the proposed DSTATCOM. The CRPWM inverter uses the error signals from the comparison results of the reference signals $\left(i_a^C\right)^*$, $\left(i_b^C\right)^*$, $\left(i_c^C\right)^*$ and the actual compensation currents i_a^C, i_b^C, i_c^C as the input. This generates the needed compensation current of the DSTATCOM for fast load compensation.

III. SIMULATION RESULTS

The Matlab/Simulink program is used for computer simulation to preliminarily verify the effectiveness of the proposed DSTATCOM. The simulation system is constructed according to Figs. 1 and 2 with the proposed compensation scheme. The circuit parameters in Fig. 1 are V_s = 220 V, L = 15 mH, f_s = 60 Hz, and C = 2,200 μF. The switching frequency of the CRPWM inverter is set at 4 kHz and the dc-link voltage is set at 500 V. The parameters of the P-I controller are obtained from a trial-and-error approach. These values are K_p = 0.35, K_i = 0.08. The simulation includes two cases:

1. Balance Load Compensation

Figure 3 shows the compensation responses of the DSTATCOM with a balance change of load. The operation point of the load is $P_{1\Phi}$ = 2,400 *W*, $Q_{1\Phi}$ = 1,800 *Var*, *PF* = 0.8 leading per-phase. At t = 0.015 s, the load is changed and the load power factor varies from 0.8 leading to 0.8 lagging. Figure 3(a) shows that, with the DSTATCOM, the source current i_a^S can be compensated to unity power factor in 3 ms. Figure 3(c) shows that when the load is capacitive, the DSTATCOM is operated in the capacitive mode. The compensation current leads the voltage by 90 degrees to supply the needed capacitive power of the load. After 0.015 s, the DSTATCOM changes to inductive mode. The compensation current lags the voltage by 90 degrees to compensate (offer) the needed inductive power. Figure 3(d) shows the variation of dc-link voltage. With the control of the P-I controller, the dc-link voltage V_{dc} is almost kept at the assigned level. Figure 3(e) shows that the reactive power from

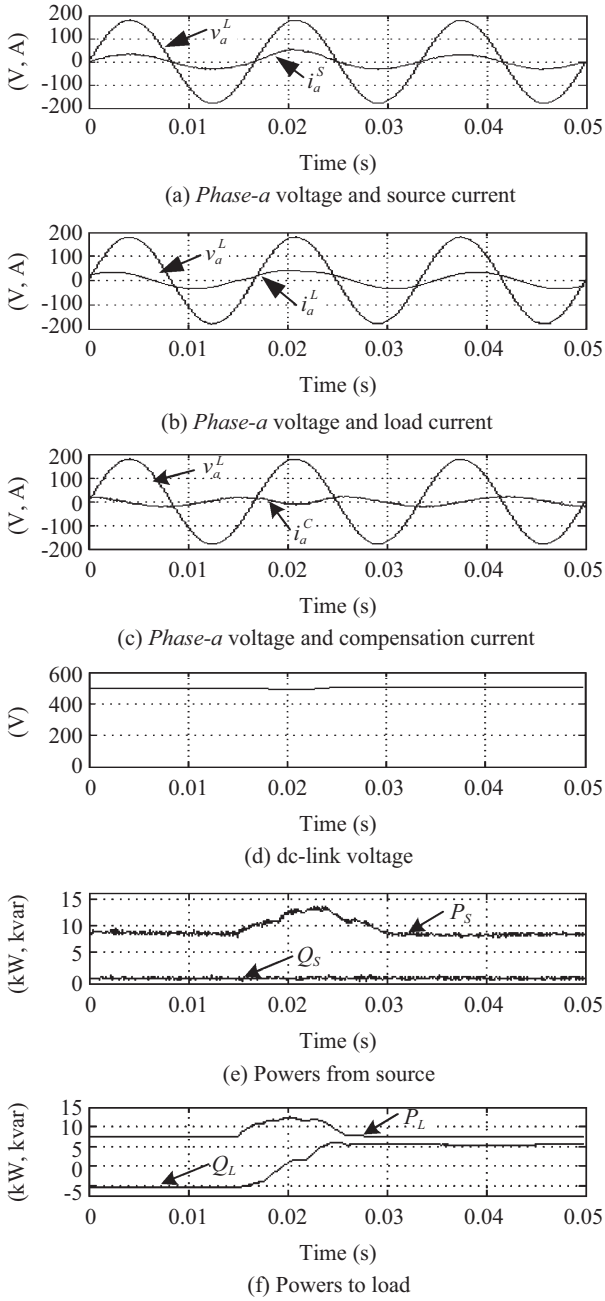

Fig. 3. Compensation responses with a change of load power factor from 0.8 leading to 0.8 lagging.

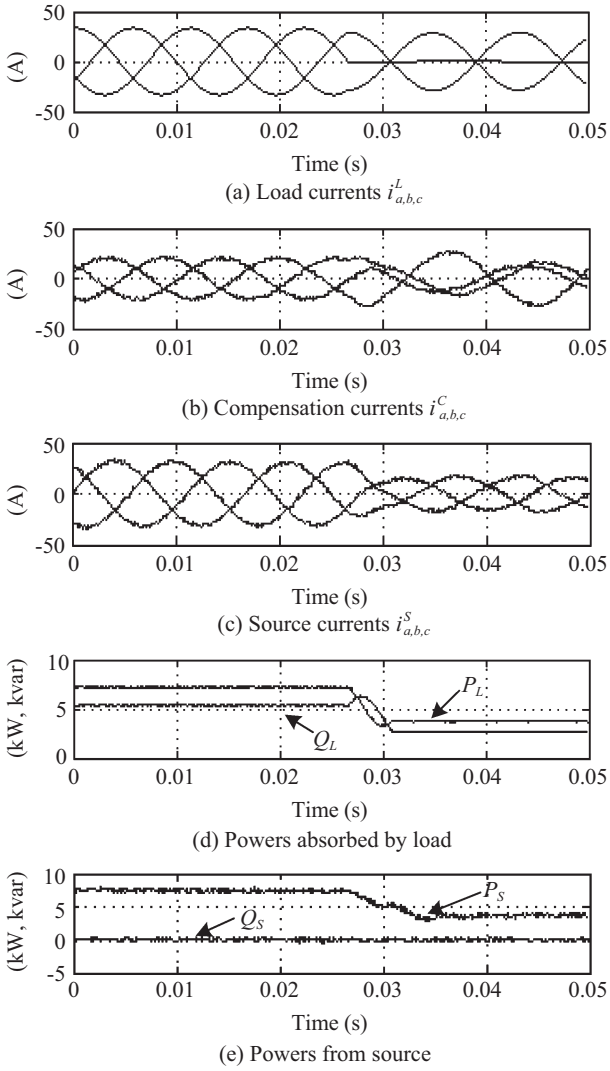

Fig. 4. Simulated transient responses with *phase-a* opened.

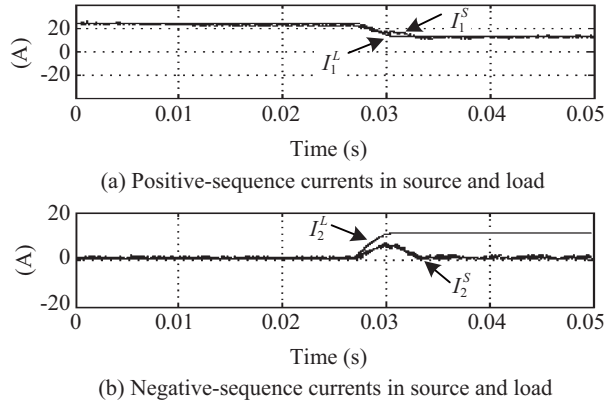

Fig. 5. Responses of positive- and negative-sequence currents during *phase-a* opened.

the power source is always zero during the compensation interval. Hence, the power factor is always corrected to unity with quick compensation time. The function of the DSTATCOM for the on-sit compensation of three-phase balanced system is verified.

2. Unbalance Load Compensation

Figure 4 shows the simulated compensation response with the DSTATCOM for unbalanced load compensation. A phase-opened of load is used in the simulation for test. The system is firstly operated at a balance condition of $P_{1\Phi}$ = 2,400 *W*, $Q_{1\Phi}$ = 1,800 *Var*, and *PF* = 0.8 lagging per phase. The *phase-a* of the load is then opened suddenly at t = 0.027 s.

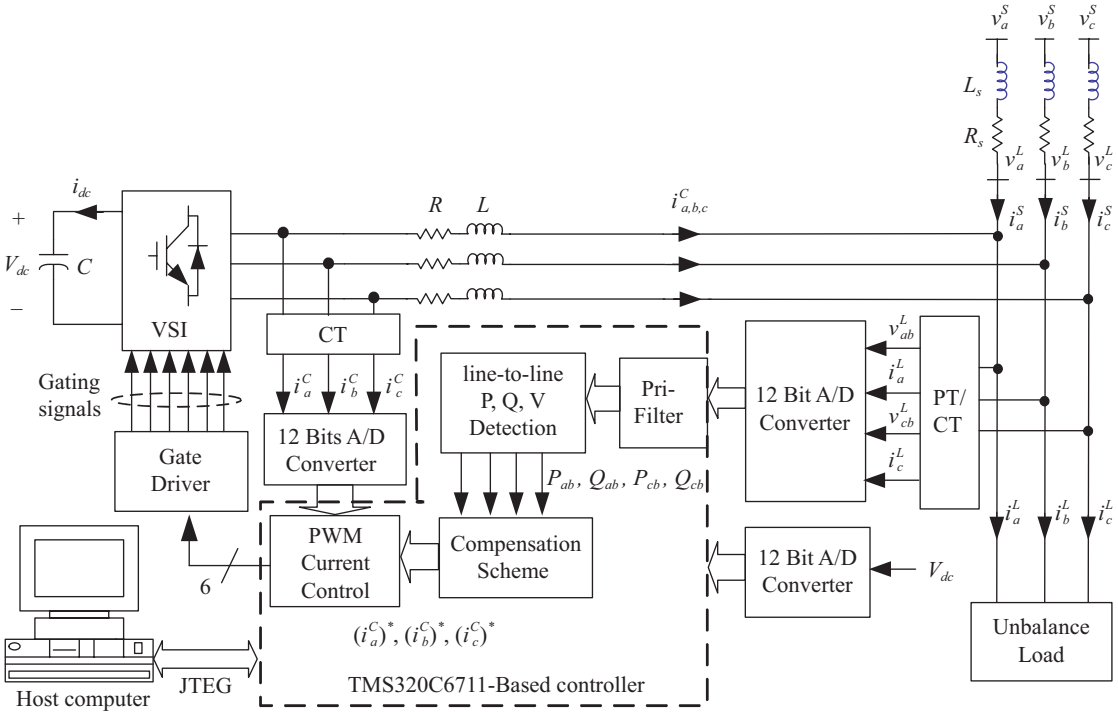

Fig. 6. Block diagram of the hardware prototype DSTATCOM.

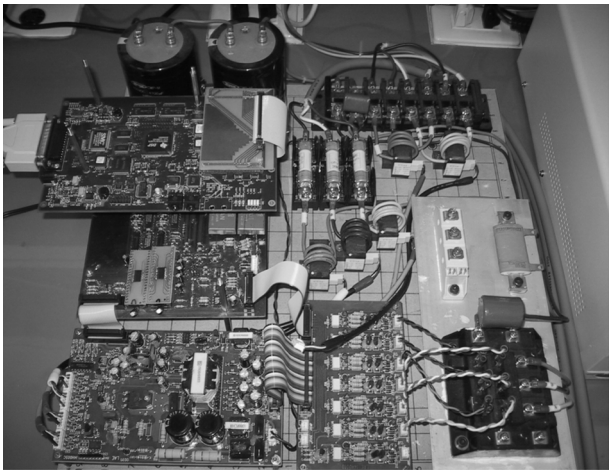

Fig. 7. Hardware prototype of the proposed DSTATCOM.

This creates an unbalanced loading condition that can be clearly observed in Fig. 4(a). Very quickly following the load change, the DSTATCOM generates the needed compensation current, as show in Fig. 4(b). Figure 4(c) shows that the source current $i^S_{a,b,c}$ are compensated to balance. Although the unbalanced load still needs reactive power, as shown in Fig. 4(d), the reactive power from the source always keeps at zero, as shown in Fig. 4(e).

Figure 5 shows the simulated positive- and negative-sequence load currents and source currents. The DSTATCOM needs only 4 ms to finish the load compensation. The response of the DSTATCOM is quick and accurate. The simulation results preliminary verifies the functions of the proposed DSTATCOM.

IV. HARDWARE IMPLEMENTATION

Figure 6 shows the block diagram for the hardware implementation of the proposed DSTATCOM by using a floating-point DSP TMS320C6711-based system. The execution program of the controller is firstly developed in the host computer with a mixed form of C language and assembly language. Then the completed execution file is downloaded to the target DSP via a data link. Use of the floating-point handling ability of the DSP easily implements the compensation scheme. The execution time is fast enough for the real-time control of the DSTATCOM.

Figure 7 shows the DSTATCOM hardware prototype setup. The circuit parameters in Fig. 6 are V_s = 220 V, L = 15 mH, R = 0.1 ohm, f_s = 60 Hz, C = 2,200 μF. A Y-connected load box is used for the experiment. A CRPWM inverter is employed for the power stage of the DSTATCOM. The switching frequency of the CRPWM inverter is 5 kHz. The dc-link voltage in the inverter is set at 500 V. The P-I voltage controller parameters are K_p = 0.35, K_i = 0.08.

In the experiment, the load is initially set at balance with a lagging power factor. The DSTATCOM in this phase is merely for power factor correction. Then, a phase-opened operation creates an unbalanced loading condition. The DSTATCOM now operates for load balancing and power factor correction.

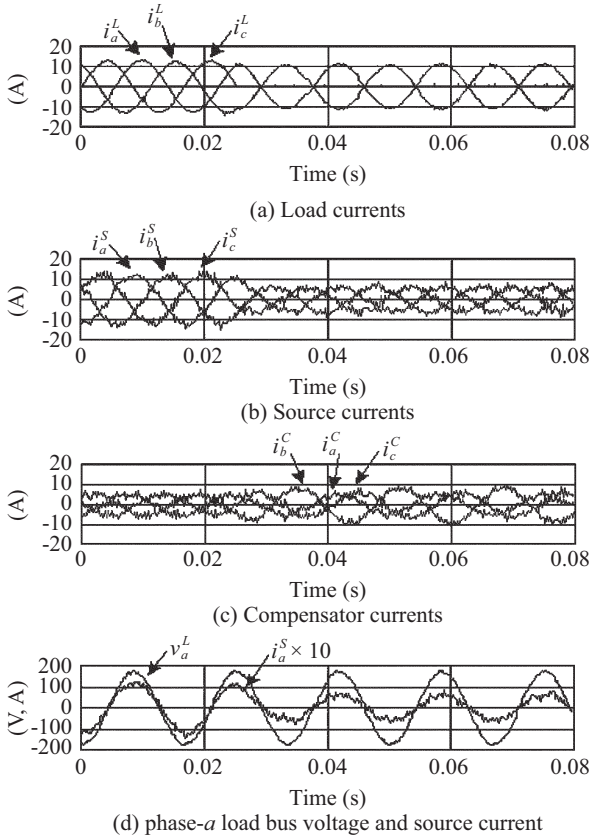

Fig. 8. Experimental results for a phase-opened operation in the load.

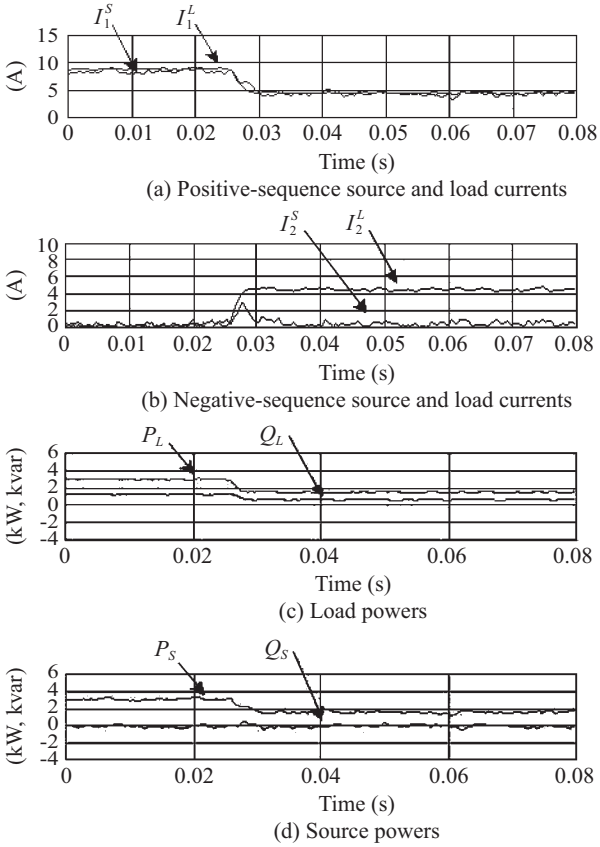

Fig. 9. Experimental results for a phase-opened operation in the load.

During the test, the instantaneous three-phase current and voltage waveforms in the load, source, and compensator sides are fetched and sent to the DSP-based controller. These data are used for the real-time calculation of the compensation scheme proposed in the paper. The generated compensation current signals are then sent to the CRPWM inverter to generate the needed compensation current. During the compensation, the controller also calculates the positive- and negative-components of load and source currents at the same time. The load and source powers are obtained. Then, the host computer fetches the calculation results via the data link in real-time to verify the compensation effect of the DSTATCOM.

Figures 8 and 9 show the experimental results. Actual current waveforms in the experiment are recorded in Fig. 8. The DSTATCOM controller calculates some useful current and power data for verifications, as shown in Fig. 9. Figures 8(a)-(c) show the measured three-phase load, source, and compensator currents when the phase-opened operation is made. Figure 8(d) shows the measured phase-*a* load bus voltage and source current with the DSTATCOM compensation. The resulting THDs of the source currents are about 7.08%, which can be improved by using well-tuned filters. Figure 9(a) shows the calculated positive-sequence source and load currents. Figure 9(b) shows the calculated negative-sequence source and load currents which reveals that, with the DSTATCOM compensation, the source current is compensated to balance within 4 ms. Figures 9(c)-(d) show that the load power factor is always kept at unity before and after the change of load. The experimental results fully match the simulation results, as shown in Figs. 4 and 5. The experimental results show that the compensation of the DSTATCOM is quick and accurate.

V. CONCLUSION

Improvement of power quality has become an important scenario in recent years. This paper has proposed the design and implementation of a DSTATCOM for the fast load compensation of three-phase three-wire unbalanced loads. For fast response requirement, a new feedforward compensation scheme is employed with symmetrical components method. In this way, the modeling and control of DSTATCOM is very similar with that of the SVC. Hence, the existing understanding of SVC remains useful. Simulation results with the program Matlab/Simulink show that the proposed DSTATCOM has very quick response time and accurate compensation effect. Accordingly, a hardware prototype employing a novel TMS320C6711 floating-point DSP-based system is then built for the final verification test. Experimental results show that the proposed DSTATCOM is very suitable for fast load com-

pensation. Compared to existing SVC, DSTATCOM has less space demand, higher response time, and generates lower noise. It is expected that DSTATCOMs will gradually replace widely used static var compensators in the near future.

NOMENCLATURE

General

Im	= imaginary part
Y	= admittance
Z, R, L	= impedance, resistance, inductance
P, Q	= active, reactive power
V, I	= phasor voltage, current
v, i	= instantaneous voltage, current
K_p, K_i	= P-I controller gain
α	= $e^{j2\pi/3}$
$\lvert\ \rvert$	= magnitude
Δ	= diviation

Superscripts

L	= load
S	= source
C	= compensator

Subscripts

a, b, c	= phase a, b, c
ab, bc, ca	= line a-b, b-c, c-a
r	= real (active) component
0, 1, 2	= zero-, positive-, negative- components
dc	= direct current
ll	= line-to-line
*	= complex conjugate or reference command

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