Journal of
Marine Science and Technology

Volume 21 | Issue 1 Article 11

# A HIGH FIGURE-OF-MERIT LOW PHASE NOISE 15-GHz CMOS VCO

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## Acknowledgements

The authors would like to thank the National Chip Implementation Center (CIC) in Taiwan for technical supports and chip fabrication in TSMC CMOS process.

Journal of Marine Science and Technology, Vol. 21, No. 1, pp. 82-86 (2013)
DOI: 10.6119/JMST-011-1230-1

# A HIGH FIGURE-OF-MERIT LOW PHASE NOISE 15-GHz CMOS VCO

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Key words: figure-of-merit, phase noise, VCO, tuning range.

## ABSTRACT

A monolithic inductor-capacitor tank (LC-tank), voltage-controlled oscillator (VCO) with high figure-of-merit (FOM), low phase noise, and low power consumption is presented for Ku-Band applications. The p-type metal-oxide-semiconductor (PMOS) differential cross-coupled topology is adopted in this design to reduce the phase noise. The measured phase noise at 1 MHz offset is -116.6 dBc/Hz at the frequency of 15.57 GHz. The excellent FOM is -192.66 dBc/Hz and the power dissipation is 6 mW. The tuning range is approximately 290 MHz with control voltage of 0 to 1.8 V. The chip size is $0.51 \times 0.74$ mm$^2$. The VCO was implemented in the Taiwan Semiconductor Manufacturing Company (TSMC) 0.18 μm complementary metal-oxide-semiconductor (CMOS) process.

## I. INTRODUCTION

Recent growth in wireless communication has led to an increasing need for transceiver circuits that are fully integrated into a single chip. The crucial design considerations of these wireless communication integrated circuits are low power consumption, low noise, and low cost. New wireless standards have been raised to higher frequencies to meet growing demand and avoid overcrowding of radio transmission. In recent years, satellite communication has made significant progress, especially in the direct broadcast satellite frequency band of 12~18 GHz [10], which is in the Ku-band range of microwave spectrum.

A voltage controlled oscillator (VCO) is one of the crucial building blocks of wireless communication transceivers. It is still a significant challenge to implement the very high frequency VCO in complementary metal-oxide-semiconductor (CMOS) technology with the limited cut-off frequency of the transistor. The difficulties in designing VCOs are to simultaneously meet different performance requirements, which include power consumption, tuning range, phase noise, and output power. Along with theses requirements, a figure-of-merit (FOM) is widely adopted to identify the characteristics of the VCO.

Many VCOs implemented by the CMOS process technology have been reported to achieve low phase noise, low power consumption, and relatively higher frequency. The most common VCO architectures are cross-coupled LC-tank structures which include n-type metal-oxide-semiconductor (NMOS) only [3], PMOS only [8], or complementary crossed-coupled pairs [2]. The LC-tank crossed-coupled VCO has the advantages of simplicity, differential operation and low phase noise. A passive inductor with high quality factor Q was used to meet the strict phase noise requirement. However, the trend towards fully integration and low cost requires the inductor to be implemented monolithically.

In this study, we propose a simple PMOS differential cross-coupled VCO with a capacitive-feedback buffer for Ku-band wireless communication applications. We successfully fabricate the VCO in the Taiwan Semiconductor Manufacturing Company (TSMC) 0.18 μm CMOS process. The measured phase noise is -116 dBc/Hz at 1 MHz offset from 15.57 GHz. The excellent FOM is -192.1 dBc/Hz and the power dissipation is 6 mW. The tuning range is about 290 MHz with control voltage of 0-1.8 V.

## II. CIRCUITT DESIGN

The proposed circuit schematic of the PMOS differential cross-coupled and the equivalent small-signal model for the VCO are illustrated in Fig. 1. The circuit shown in Fig. 1 has the following transfer function which can be expressed as:

$$\frac{v_o(s)}{v_i(s)} = \frac{s g_m L_T}{s^2 L_T C_T + \frac{s L_T}{R_T}(1 - A_v) + 1} \tag{1}$$

$$s_1, s_2 = -\left(\frac{1 - A_v}{2 R_T C_T}\right) \pm j\sqrt{\frac{1}{L_T C_T} - \left(\frac{1 - A_v}{2 R_T C_T}\right)^2} \tag{2}$$

$$|s_1| = |s_2| = \sqrt{\frac{1}{L_T C_T}} = \omega_0 \tag{3}$$

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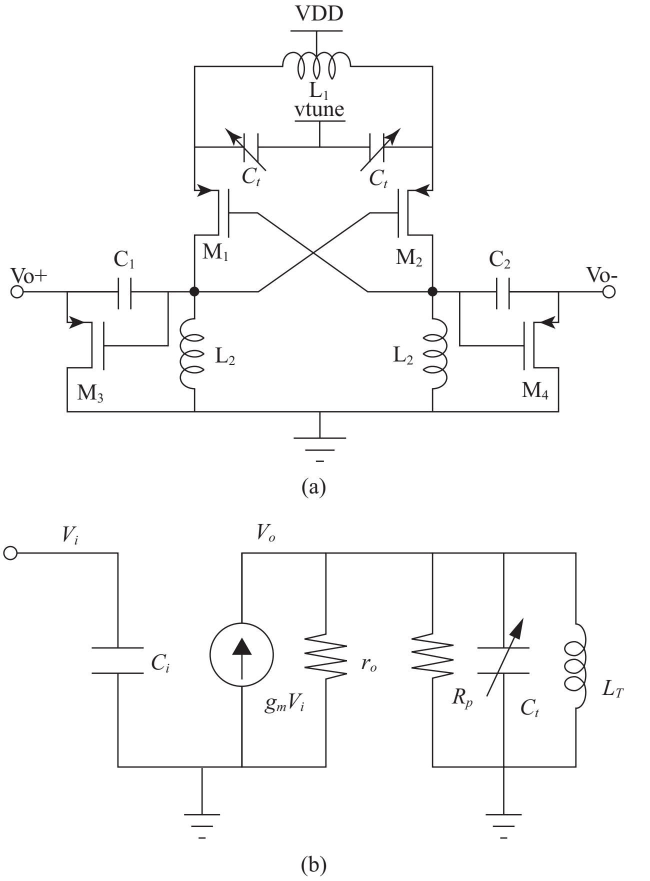


**Fig. 1. (a) The schematic of the proposed VCO and (b) the equivalent small-signal model.**

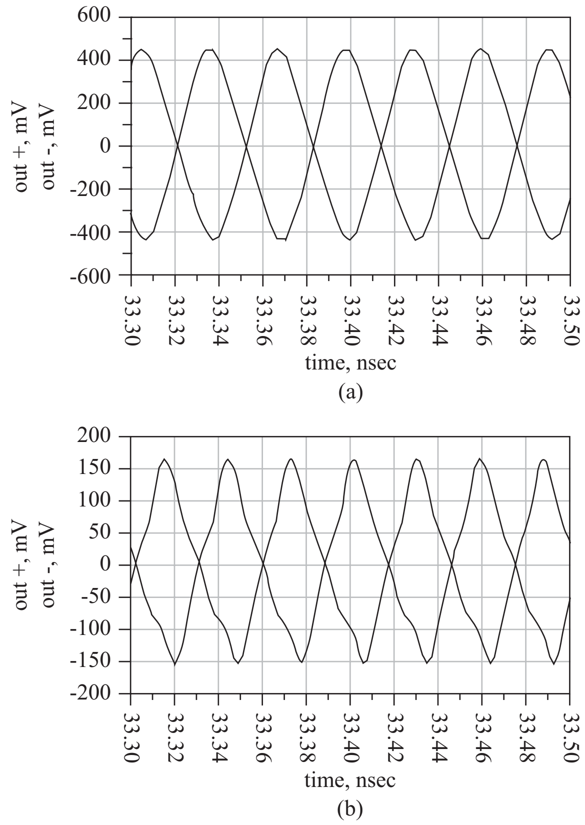


**Fig. 2. Simulation of $C_1$ and $C_2$ (a) with capacitive feedback and (b) without capacitive feedback.**

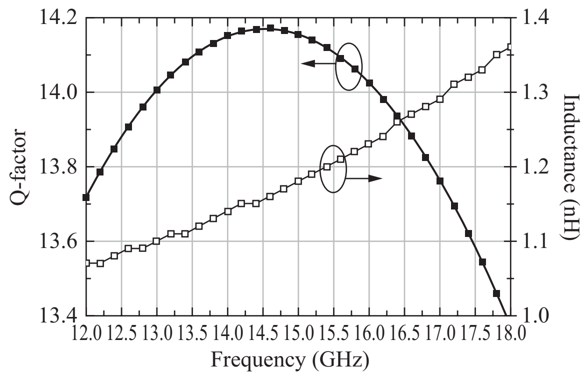


**Fig. 3. Simulated quality factor and inductance versus frequency of $L_1$.**

where $L_T = (L_1/2)//L_2$, $R_T = r_o//R_p$, $C_T = C_{sg} + C_{dg} + C_t$, and $A_v = g_m R_T$. The circuit is designed using the Advanced Design System (ADS) and Momentum Electromagnetic (EM) simulator. The circuit is constructed using only PMOS transistors, due to the lower flicker noise of PMOS transistors as compared to NMOS transistors [5]. $L_1$ replaces the traditional transistor current source in order to increase the voltage swing. $L_2$ and $C_t$ form the main resonator to obtain the oscillation frequency and tuning range. $M_1$ and $M_2$ are crossed-coupled pairs that provide negative resistance to compensate for the parasitic impedance of inductors and capacitors. The transistor sizes of $M_1$ and $M_2$ are 45 μm and 0.18 μm, respectively. Transistors ($M_3$ and $M_4$) and capacitors ($C_1$ and $C_2$) are the buffer. $C_1$ and $C_2$ form the capacitive feedback to improve the phase noise and linearity. $C_1$ and $C_2$ forming the capacitive feedback are designed to improve the output swing performance which is shown in Fig. 2. From the figure, we can obtain that with capacitive feedback structure, the output swing is increased.

The on-chip inductor plays an important role in the characteristics of VCO. Improving the Q-factors of the inductors can reduce phase noise and power consumption. In order to gain the center frequency in the Ku-band range, we simulate the inductance and Q-factor of $L_1$ from 12 GHz to 18 GHz. $L_1$ is symmetrical with the center tapped inductor. Fig. 3 illustrates the characteristics of inductance and quality factor Q versus frequency. At an approximate frequency of around 15.5 GHz, the quality factor of $L_1$ is 14.09 and the inductance value is 1.21 nH. We use a standard inductor for $L_2$. Fig. 4 illustrates the simulated inductance and quality factor versus frequency characteristics of $L_2$. The inductance of $L_2$ is 234.1 pH and the quality factor is 19.62 at 15.5 GHz.

A key component in the design of VCO is a varactor, used

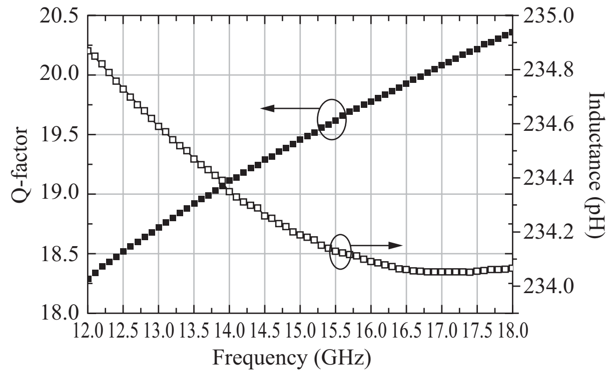


**Fig. 4. Simulated quality factor and inductance versus frequency of $L_2$.**

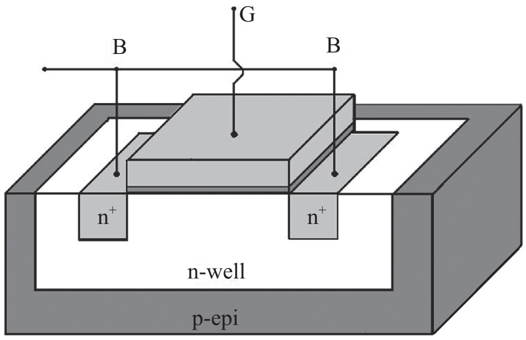


**Fig. 5. Cross section of a MOS varactor.**

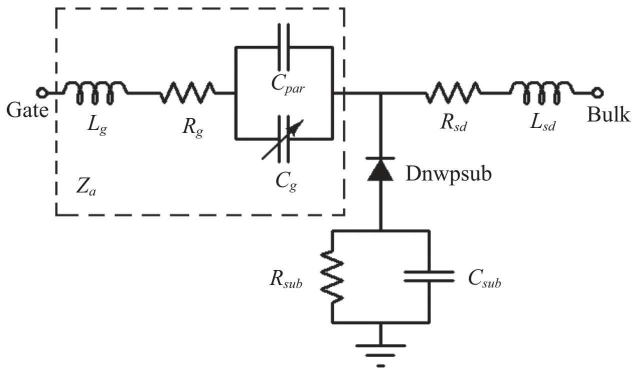


**Fig. 6. Equivalent circuit model of the varactor.**

to determine the performance of the tuning range. We used the accumulation-mode MOS varactor in our design, as it has better performance than an inversion-mode MOS varactor and diode varactor [1]. The cross section of the accumulation-mode MOS varactor is illustrated in Fig. 5. The varactor has two terminals: G and B. The variable capacitance is controlled by the gate voltage. The equivalent model of varactor is illustrated in Fig. 6 [11]. The impedance $Z_a$ is defined as (neglecting $C_{par}$)

$$Z_a = R_g + \frac{1}{j\omega C_g} + j\omega L_g \tag{4}$$

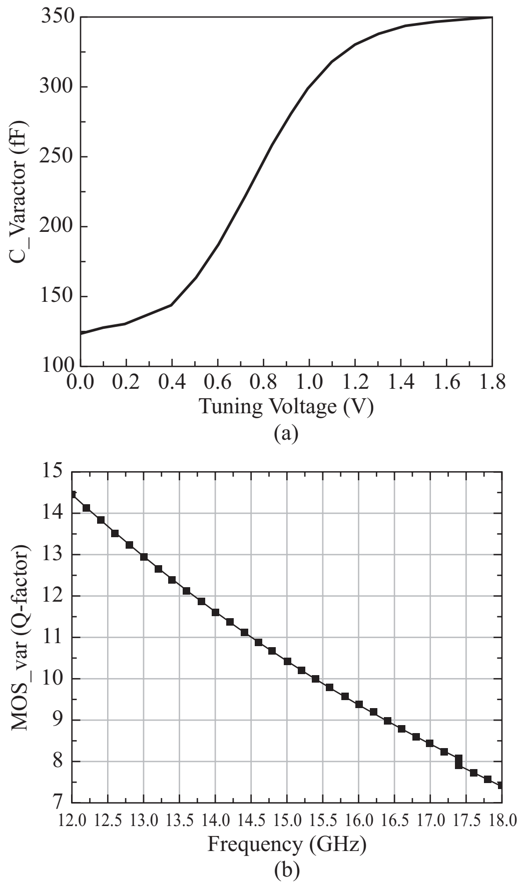


**Fig. 7. (a) Simulated $C_t$ capacitance versus tuning control voltage, and (b) quality factor of $C_t$ versus frequency.**

$L_g$ is the ploy gate and vias parasitic inductance. $C_g$ is the variable capacitance of the MOS varactor. $R_g$ is the gate and channel parasitic resistance. $C_{par}$ is the parasitic capacitance of the MOS varactor. Dnwpsub is the diode between N-well and P-substrate. $R_{sub}$ and $C_{sub}$ are P-substrate resistance and P-substrate capacitance. $R_{sd}$ is the parasitic resistance connected to the bulk. $L_{sd}$ is the bulk and vias parasitic inductance.

Capacitance and quality factor are, respectively, obtained from the following equations:

$$C_g = \left|\frac{1}{\omega^2 L_g - \omega I_m(Z_a)}\right| \approx \left|\frac{1}{\omega I_m(Z_a)}\right| \tag{5}$$

The $\omega^2 L_g$ is insignificant and neglected from the equation.

$$Q_C \equiv \frac{\text{Power storage}}{\text{Power consumption}} = \left|\frac{I_m(Z_a)}{R_e(Z_a)}\right| \tag{6}$$

For varactor simulation the bulk terminal is biased at 1.8 V. MOS varactor capacitance ($C_t$) versus tuning control voltage curve is shown in Fig. 7(a). The MOS varactor

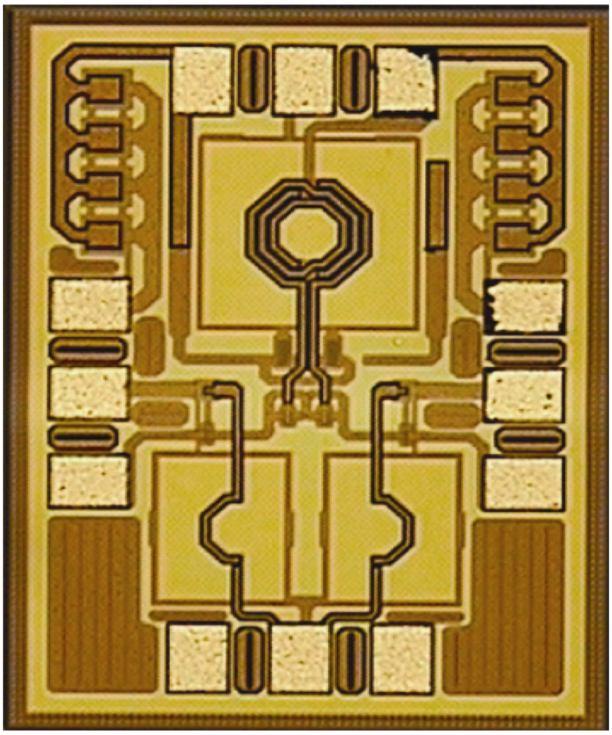

**Fig. 8. Chip microphotograph of the VCO.**

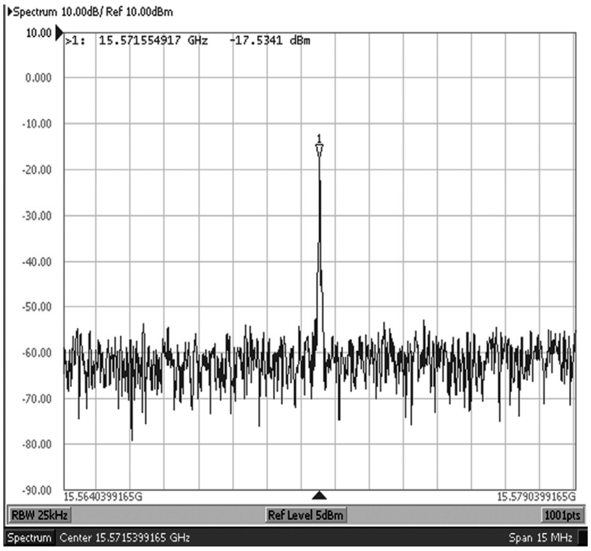


**Fig. 9. Measured output spectrum of the VCO.**

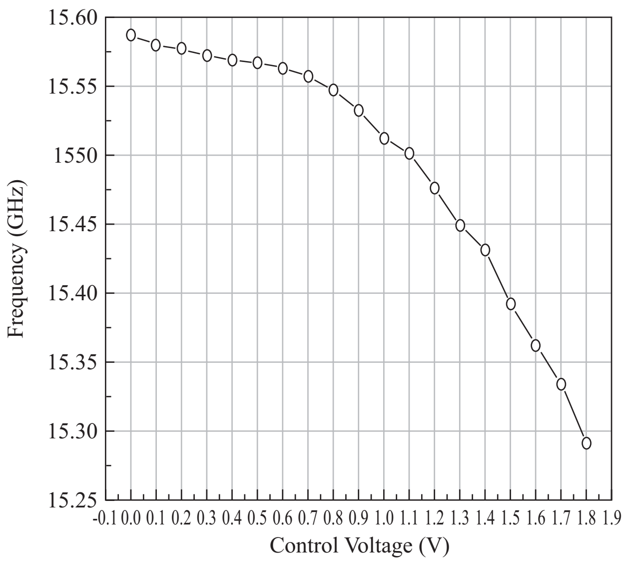


**Fig. 10. Measured tuning range characteristics of the VCO.**

capacitance value varies from 123.9 fF to 350 fF when the control voltage is changed from 0 V to 1.8 V. Fig. 7(b) shows the varactor's Q value as a function of frequency, where its value is about 10 at 15.5 GHz. The capacitive feedback topology is added with the cross-coupled pairs to suppress the parasitic effect caused by transistors. The oscillator frequency can be determined by Eq. (7).

$$f_{OSC} = \left(2\pi\sqrt{L_T\left(C_T + C_{ind} + C_{MOS}\right)}\right)^{-1} \tag{7}$$

where $C_T$ is the equivalent capacitance of one varactor, $C_{ind}$ is the equivalent parallel capacitance of the inductor, and $C_{MOS}$ is the equivalent parallel capacitance of the PMOS cross-coupled transistor.

## III. MEASUREMENT RESULTS

The chip photograph is shown in Fig. 8. The chip area is $0.51 \times 0.74$ mm$^2$ including RF pads. The measurements of VCO parameters, including output spectrum, and output power are performed by the Agilent E5052A spectrum analyzer, operating at a supply voltage of 1.8 V, the core current of 3.33 mA, and power consumption of 6 mW. Fig. 9 illustrates the output spectrum and the output power. As the measured output power cable loss compensation is 3 dB at 13~16-GHz, the output power is -14.53 dBm at 15.57 GHz. Fig. 10 illustrates the measured tuning frequency versus the varactor control voltage. The oscillation frequency ranges from 15.58 GHz to 15.29 GHz with a tuning range of approximately 290 MHz for control voltage, varying from 0 to 1.8 V. The measured phase noise is -116 dBc/Hz at 1 MHz offset frequency from 15.57 GHz, as shown in Fig. 11.

The FOM of VCO performance is defined as [6]:

$$\mathrm{FOM} = L\{f_{offset}\} - 20\cdot\log\left(\frac{f_0}{f_{offset}}\right) + 10\cdot\log\left(\frac{P_{DC}}{1\,mW}\right) \tag{8}$$

$L\{f_{offset}\}$ is the phase noise in dBc/Hz at offset frequency $f_{offset}$ from the carrier frequency $f_0$. $P_{DC}$ is the DC power dissipation in mW. In this Ku-band VCO, the FOM at 1 MHz offset frequency is about -192.1 dBc/Hz. Table 1 lists the performance of the proposed VCO compared to other reported VCOs in a similar frequency range.

**Table 1. Performance comparison.**

| | Freq. (GHz) | Phase Noise (dBc/Hz) | FOM (dBc/Hz) | Tuning Range (MHz) | $P_{DC,\mathrm{core}}$ (mW) | Chip size (mm$^2$) |
|---|---|---|---|---|---|---|
| [12] | 16 | -111 | -186.8 | 900 | 8.1 | 0.365 |
| [7] | 16.5 | -115 | -188.4 | 870 | 12.6 | 0.588 |
| [9] | 11.6 | -110.8 | -183 | 630 | 8.1 | 0.45 |
| [4] | 15 | -112.2 | -178.6 | 250 | 52 | 1.1 |
| This work | 15.57 | -116.6 | -192.7 | 290 | 6 | 0.377 |

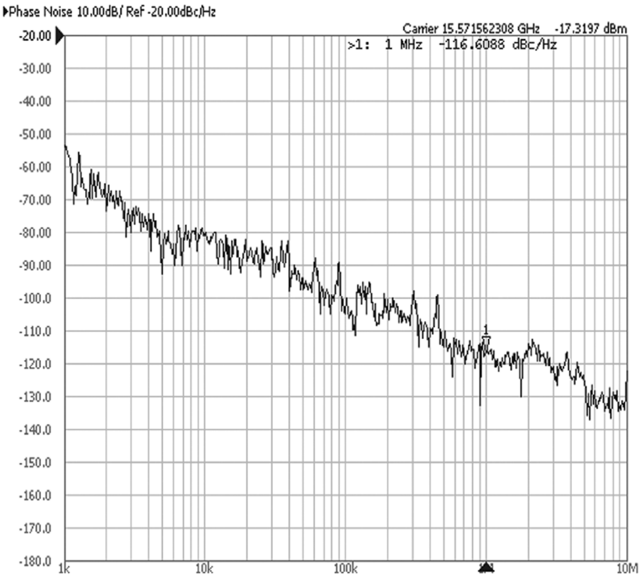


**Fig. 11. Measured phase noise performance of the VCO.**

## IV. CONCLUSION

In this article, a Ku-band fully integrated crossed-coupled differential voltage-controlled oscillator is presented. The VCO is successfully fabricated in TSMC CMOS 0.18 μm 1P6M process. The measured tuning range is from 15.58 GHz~15.29 GHz with control voltage from 0 to 1.8 V. The measured phase noise is as low as -116.6 dBc/Hz at 1 MHz offset from 15.57 GHz and the FOM is good to -192.66 dBc/Hz. The power consumption of the VCO core is 6 mW.

## ACKNOWLEDGMENTS

The authors would like to thank the National Chip Implementation Center (CIC) in Taiwan for technical supports and chip fabrication in TSMC CMOS process.

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