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Jium-Ming Lin
Dept. of Communication Engineering, Chung-Hua University, Hsin-Chu, Taiwan, R.O.C, jmlin@chu.edu.tw

Yuan-Jung Chiang
Dept. of Electrical Engineering, Chung-Hua University, Hsin-Chu, Taiwan, R.O.C.

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A NOVEL METHOD FOR TESTING LCD BY INTEGRATING SHORTING BAR AND TAGUCHI DOE TECHNOLOGIES

Jium-Ming Lin[1] and Yuan-Jung Chiang[2]

Key words: line defect, parameter design, false defect, point defect, thin-film transistor (TFT), LCD.

ABSTRACT

This paper proposes a novel LCD false defect detection method that involves integrating shorting-bar and Taguchi technologies. When both the gate and data lines of an LCD are activated using a shorting bar technique, and an illuminator is applied to the background panel, if all thin-film transistor (TFT) arrays are free of point defect failures, then the lights from the illuminator can penetrate the scanned pixels (i.e., a bright, complete image should appear on the display). Otherwise, there are defects in the TFT cells exhibiting dark patterns. In this study, the P-diagram of the Taguchi design of experiment method was integrated to simplify the conditions for the TFT tester design. The resulting real defect ratio is increased by 90%, whereas the false defect ratio is increased by only 0.34%. Notably, the line defect location accuracy can also be increased by adding special runs to the corresponding test waveforms and patterns.

I. INTRODUCTION

In recent years, TFT manufacturing technologies have demonstrated substantial improve mentsim provements (Henly and Barton, 1992, 2002; Jenkins et al., 1992; Lalama, 1994; Oshimi, 1995; Aoki, 1998; Bosacchi, 2000; Yang, 2001; Crawford, 2005; Wang, 2010). The size of glass substrates has steadily increased according to production rates and fields of application. However, because the increase size of glass substrates has generated higher production costs, the most crucial factor in reducing these costs is the yield. Thus, one should increase the detection rates of defects and faults. This paper proposes a novel LCD defect detection method that involves integrating shorting bar and Taguchi technologies (Lalama, 1994; Hsieh and Lu, 2008; Lin et al., 2009; Wang, 2010; Liu et al., 2013). The Taguchi design of experiment (DOE) method is used to determine the key parameters for the TFT tester design (Hsieh and Lu, 2008; Lin et al., 2009; Liu et al., 2013). Note that the simplified test parameters and conditions enable finding 90% of the faults, whereas the false defect ratio is increased by only 0.34%. Furthermore, the line defect location accuracy can also be increased by adding special runs to the corresponding test waveforms and patternshus, the proposed method can provide a higher yield rate, lower production cost, and greater productivity. The remainder of this paper is organized as follows: Section I introduces the proposed method. Section II addresses system operation principles and tester structures. The Taguchi DOE method is described in Section III, and Section IV discusses the relevant improvements. Finally, Section V presents the conclusion.

II. SYSTEM OPERATION PRINCIPLES AND TESTER STRUCTURES

1. Array Tester

The operation principles and structures of the stage, probe frame, and array tester are desscribed as follows:

(1) Stage: Composed of ceramic to support the glass substrate, thereby reducing the forces of electrostatic attraction and the vacuum adherence effect between the substrate and the stage during pick-and-place and preventing substrate breakage.
(2) Probe frame: A test fixture with probe pins to connect the input and output signals to TFT arrays.
(3) Voltage imaging optical system (VIOS): The array tester, which consists of an optical modulator, charge-coupled device (CCD) camera, and illuminator. The illuminator provides light to penetrate the modulator. The modulator has three layers and replaces the liquid crystal. The first layer consists of indium tin oxide-coated Mylar, connecting the modulator gate bias voltages to the TFT arrays. The second layer consists of liquid crystal for testing the

Paper submitted 02/23/14; revised 05/07/15; accepted 11/12/15. Author for correspondence: Jium-Ming Lin (e-mail: jmlin@chu.edu.tw).
[1] Dept. of Communication Engineering, Chung-Hua University, Hsin-Chu, Taiwan, R.O.C.
[2] Dept. of Electrical Engineering, Chung-Hua University, Hsin-Chu, Taiwan, R.O.C.

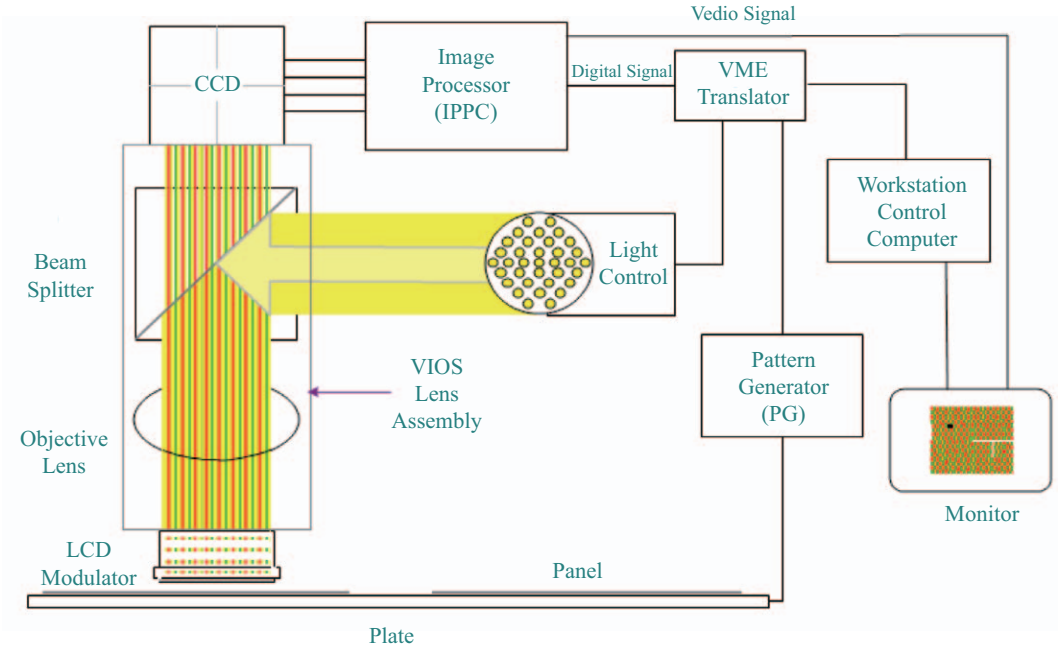


Fig. 1. Block diagram of tester operation principle.

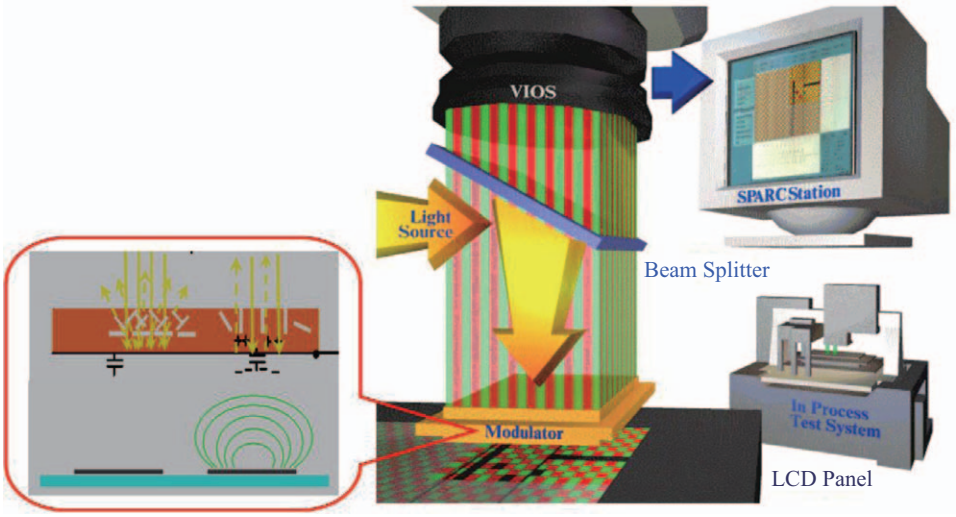


Fig. 2. TFT defect detection principle.

TFT arrays, and the third layer is composed of metal and acts as a pellicle mirror at the bottom of the modulator to reflect the light. The CCD camera captures the LCD image to validate the function of the TFT arrays. The optical modulator is positioned beneath the VIOS to align it with the CCD camera.

2. Tester Operation Principles

The block diagram of the tester is shown in Fig. 1. The input voltage and current from the probe frame are applied to TFT arrays for testing. The bias voltages are then applied to the modulator to establish electric fields between the mirror and the TFT arrays [3]. Thus, the liquid crystal can be twisted to reflect the light from the illuminator for the CCD camera taking the images. The image signals are then transmitted to an IPPC (image processor) to convert the brightness into voltage signals. If the resulting voltage is above the upper threshold value or below the lower threshold value, then the TFT pixel is abnormal and with defect. Note that one can optionally use a defect review camera to examine the defect mode and uplink it to the corresponding server for use in subsequent laser repair.

3. Principle of TFT Defect Detection with Modulator

The TFT defect detection principle is shown in Fig. 2. If the electric field does not exist between the modulator and TFT substrate, then the incident light from the illuminator cannot

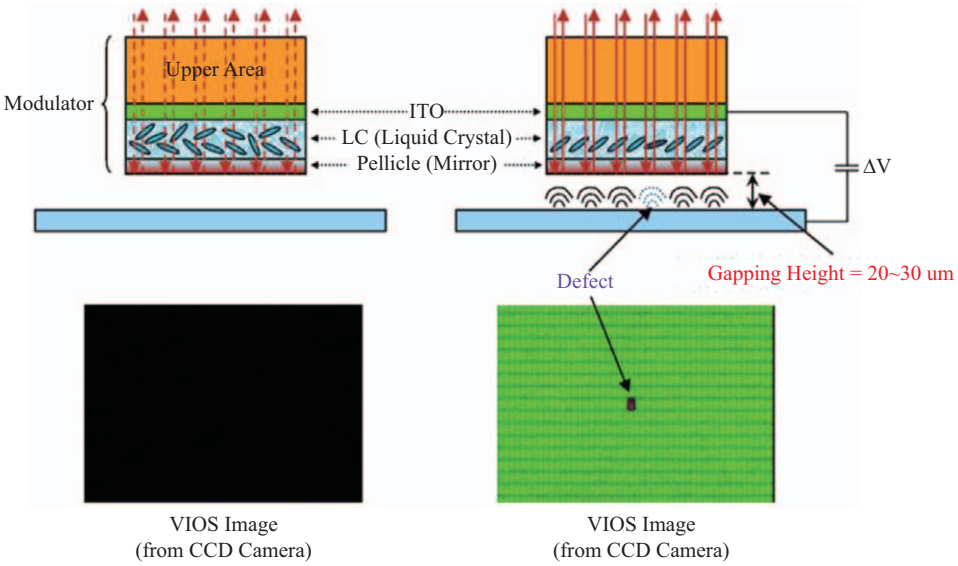


Fig. 3. Cases with and without electric field.

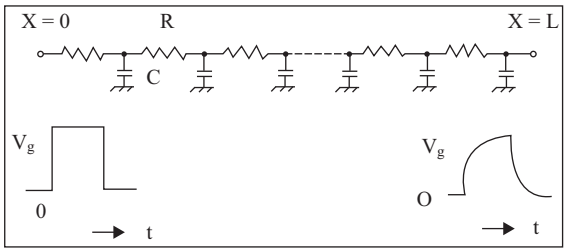


Fig. 4. Equivalent RC delay diagram of gate line.

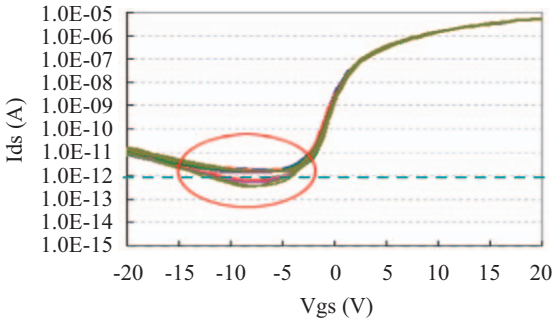


Fig. 5. Expanded Ioff may cause a false defect.

pass through the modulator; therefore, the CCD brightness is extremely low, producing a dark VIOS image, as shown on the left side of Fig. 3. Otherwise, the image color of the VIOS is green, as shown on the right side of Fig. 3.

4. False Defect Analysis

The first type of false defect is caused by a TFT gate line RC delay and loading effects for the high resolution and density requirements as time transpires. Thus, the applied gate voltage waveform near the far end has serious distortion, as shown in the equivalent circuit gate line diagram in Fig. 4. The second type of false defect is caused by an expanded TFT leakage current (Ioff), as shown in Fig. 5.

Fig. 6. Serious defect with a large area shorted.

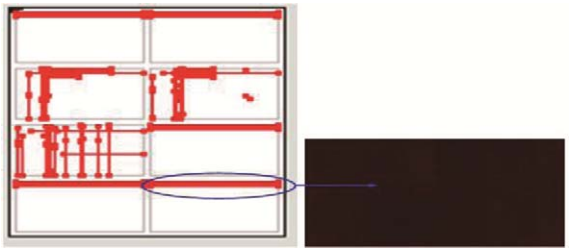


Fig. 7. Defect test map and the VIOS image (serious line defect).

5. Loss Detection of Real False Defects

The opposite effect of overscreening is the loss detection of real false defects. If one decreases the screening levels, changing the defect criteria, then the loss detection of real false defects may be increased.

6. Location of Line Defects

When a line defect is of short mode, locating the defect is difficult. The reasons are as follows:

(1) Serious line defect; large area shorted: When a large quantity of metal remains on the substrate surface after the metallization and etching processes, as shown in Fig. 6, several even and odd lines may be shorted to each other, producing a dark VIOS image, as shown in Fig, 7.

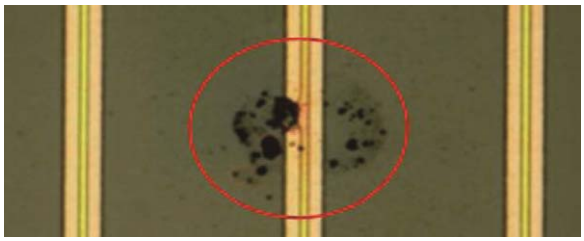


Fig. 8. Slight line defect.

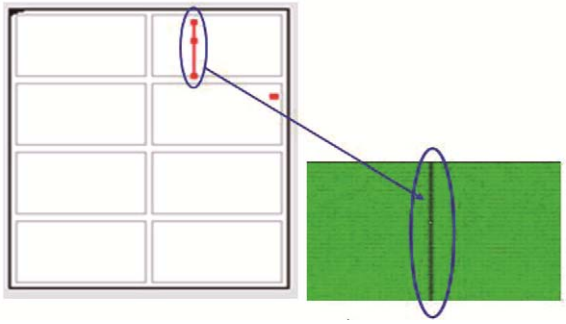


Fig. 9. Defect test map and the VIOS image (slight line defect).

(2) Slight line defect; small area shorted: When small pieces of metal remain on the substrate, as shown in Fig. 8, only a single dark line is produced, as shown in Fig. 9. However, the location of the defect in the line cannot be defined. Thus, the Taguchi DOE method is applied not only to determine the key parameters for testing TFT arrays but also to increase the accuracy of line defect location.

III. TAGUCHI DOE METHOD

The Taguchi method entails a particular DOE in which the key parameters and their respective values are sought to increase system performance while decreasing the number of tests required [11-13]. The involved steps are as follows:

(1) Define the purpose of the experiment.
(2) Confirm the ideal function/response.
(3) Choose the signal and noise factors.
(4) Choose the control factors and levels.
(5) Design the experiment.
(6) Collect the experimental data.
(7) Conduct data analysis.
(8) Propose a conclusion.
(9) Perform a conformation run.

Once these steps are completed, orthogonal arrays are constructed to find the key parameters and corresponding values, thereby reducing the number of experiments. We can then simplify complex experiments, reduce overscreening, and increase false defect detection and location capabilities. Therefore, the productivity and yield rate can be increased, and the cost of production can be reduced.

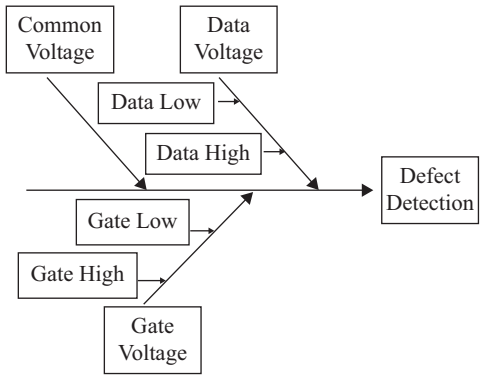


Fig. 10. Fishbone diagram of the five major factors in defect detection.

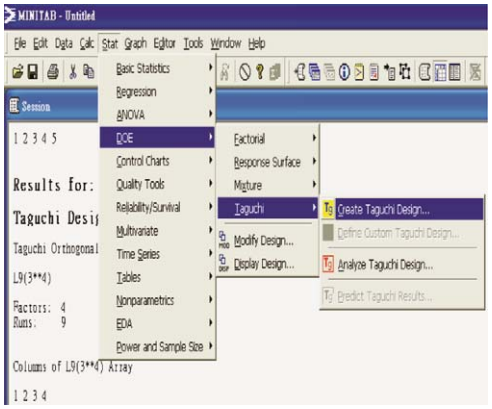


Fig. 11. Display settings pertinent to the Taguchi method.

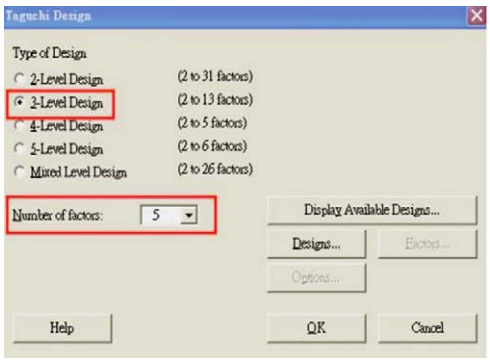


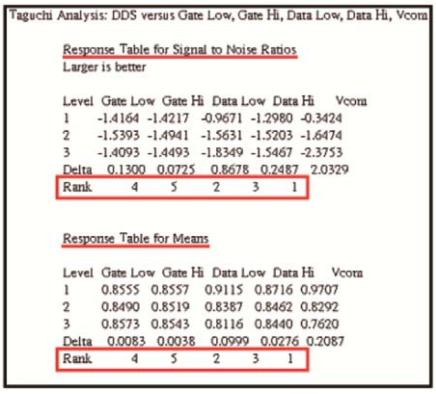
Fig. 12. Parameter settings.

1. Major Factors in Defect Detection

Major factors in defect detection, such as the voltages of gate high, gate low, data high, data low, and common (Vcom), are shown in the fishbone diagram in Fig. 10. According to the traditional test method for defect detection, the total number of test conditions for the five major factors with three levels is 243 (= 35). Therefore, it is highly difficult to perform all of the experiments required under these conditions. However, through the Taguchi method, only 27 experiments are required, as shown in Table 1. Figs. 11 and 12 show the displayed parameter settings pertinent to the Taguchi method.

Table 1. Experiments carried out using the Taguchi method and results, including SNR and DDS mean values.

Count	Gate Low	Gate High	Data Low	Data High	Vcom	Site Voltage	Defact Voltage	DDS	MEAN	SNRA
1	-15	15	-5	19	-2	7.6	1.8	0.763	0.763	-2.347
2	-15	15	-5	19	-3	6.6	1.2	0.818	0.818	-1.743
3	-15	15	-5	19	-4	6.4	0.5	0.922	0.922	-0.706
4	-15	16	-6	20	-2	6.9	1.4	0.797	0.797	-1.97
5	-15	16	-6	20	-3	8	0.6	0.925	0.925	-0.677
6	-15	16	-6	20	-4	7.1	1.6	0.775	0.775	-2.218
7	-15	17	-7	21	-2	5.5	1.2	0.782	0.782	-2.138
8	-15	17	-7	21	-3	5.2	1.1	0.789	0.789	-2.064
9	-15	17	-7	21	-4	5.5	-0.8	1.146	1.146	1.18
10	-16	15	-6	21	-2	8	1.8	0.775	0.775	-2.214
11	-16	15	-6	21	-3	7.1	1.7	0.761	0.761	-2.377
12	-16	15	-6	21	-4	6.8	0.4	0.941	0.941	-0.526
13	-16	16	-7	19	-2	7.1	2.4	0.662	0.662	-3.583
14	-16	16	-7	19	-3	6.44	0.4	0.938	0.938	-0.557
15	-16	16	-7	19	-4	6	-1	1.167	1.167	1.339
16	-16	17	-5	20	-2	6	1.7	0.717	0.717	-2.893
17	-16	17	-5	20	-3	6.8	1.4	0.794	0.794	-2.003
18	-16	17	-5	20	-4	6.2	0.7	0.887	0.887	-1.041
19	-17	15	-7	20	-2	8	1.8	0.775	0.775	-2.214
20	-17	15	-7	20	-3	7	1.2	0.829	0.829	-1.633
21	-17	15	-7	20	-4	6.8	-0.8	1.118	1.118	0.966
22	-17	16	-5	21	-2	9	2	0.778	0.778	-2.183
23	-17	16	-5	21	-3	8	1.5	0.813	0.813	-1.804
24	-17	16	-5	21	-4	7.5	1.4	0.813	0.813	-1.795
25	-17	17	-6	19	-2	6.3	1.2	0.81	0.81	-1.836
26	-17	17	-6	19	-3	6.9	1.4	0.797	0.797	-1.97
27	-17	17	-6	19	-4	6.3	0.2	0.968	0.968	-0.28



Taguchi Analysis: DDS versus Gate Low, Gate Hi, Data Low, Data Hi, Vcom

Response Table for Signal to Noise Ratios
Larger is better

Level	Gate Low	Gate Hi	Data Low	Data Hi	Vcom
1	-1.4164	-1.4217	-0.9671	-1.2980	-0.3424
2	-1.5393	-1.4941	-1.5631	-1.5203	-1.6474
3	-1.4093	-1.4493	-1.8349	-1.5467	-2.3753
Delta	0.1300	0.0725	0.8678	0.2487	2.0329
Rank	4	5	2	3	1

Response Table for Means

Level	Gate Low	Gate Hi	Data Low	Data Hi	Vcom
1	0.8555	0.8557	0.9115	0.8716	0.9707
2	0.8490	0.8519	0.8387	0.8462	0.8292
3	0.8573	0.8543	0.8116	0.8440	0.7620
Delta	0.0083	0.0038	0.0999	0.0276	0.2087
Rank	4	5	2	3	1

Fig. 13. Analysis summary.

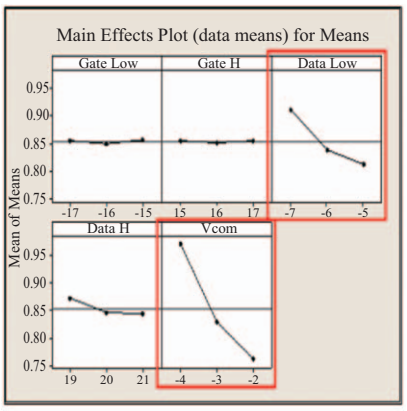


Fig. 14. Main effect plot of means.

Ten types of defects (e.g., data line shorted without an insulating layer between the data line and ground; data line shorted to the gate by a nonetched metal layer; data line opened for the unremoved photo mask) were used as samples for testing to calculate the defect detection sensitivity (DDS), defined as follows:

$$\text{DDS} = (\text{site voltage} - \text{defect voltage}) / \text{site voltage} \quad (1)$$

2. SNR and DDS Mean Value

Applying the requirement of a higher signal-to-noise ratio (SNR) is favorable. The SNRs and DDS mean values are listed in Table 1. A summary of the Taguchi analysis results, main effect plot of means, and SNRs is shown in Figs. 13, 14, and 15, respectively.

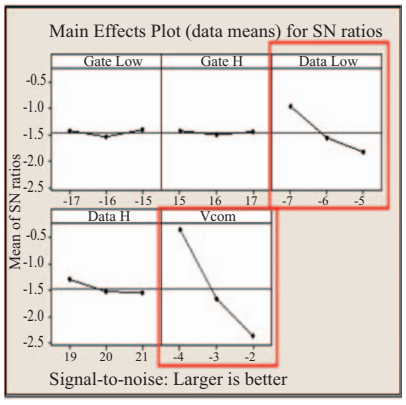


Fig. 15. Main effect plot of SN ratios.

Table 2. Erformance comparisons between original and new test waveforms and patterns.

Defect	Original pattern	New pattern
False defect count	3	6
Real defect count	40	76
Total defect count	43	82
False defect ratio	6.98%	7.32%
Real defect improve	90.00%	
False defect increasing	0.34%	

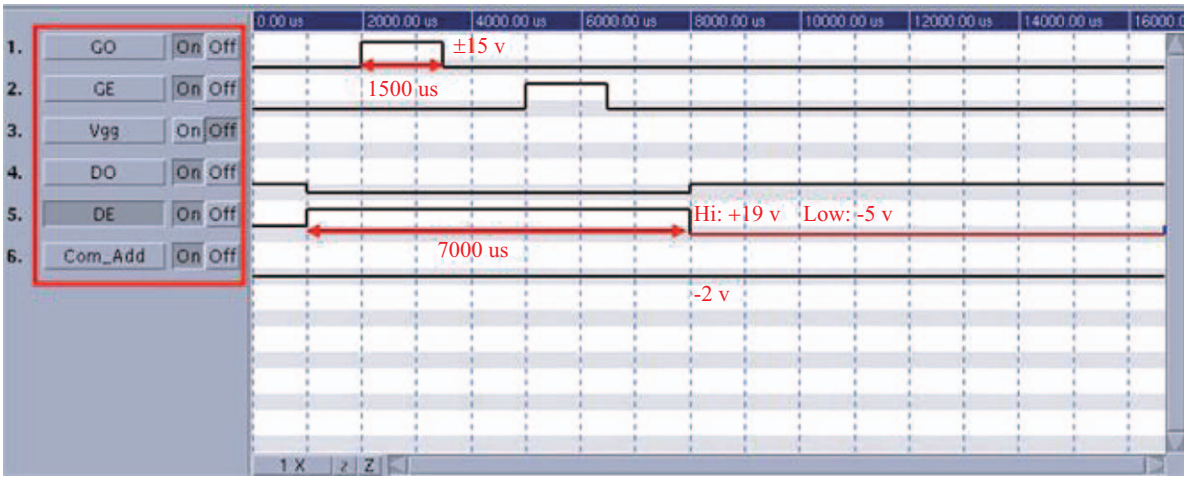


Fig. 16. Original test waveforms and patterns.

IV. IMPROVEMENTS IN OVERSCREENING AND DEFECT DETECTION

1. Performance Comparison between Original and New Test Waveforms and Patterns

The results of the performance comparison between the original and new test waveforms and patterns are listed in Table 2. Note that using the new test waveforms and patterns of Vcom and data low voltage, can increase the real defect detection performance. In addition, although the gate high voltage and gate high pulse width are not the major factors in real defect detection, they can decrease the false defect of overscreening caused by the gate line RC delay effect. The real defect ratio is increased by 90%, whereas the false defect ratio is increased by only 0.34%.

Ten TFT glass substrates were applied to verify the improvements in defect detection and reduction of overscreening after applying the Taguchi method. Each TFT glass substrate contains 1024 × 768 pixels; therefore, 10 TFT glass substrates comprise 1024 × 728 × 10 pixels; thus, the number of samples is sufficiently high for statistical analysis. The original test waveforms and patterns of the five major factors in defect detection are shown in Fig. 16 and described as follows:

(1) Gate voltage high: +15 V; low: -15 V.
(2) Pulse width: 1500 μs.
(3) Data voltage high: +19 V; low: -5 V.
(4) Pulse width: 7000 μs.
(5) Common voltage: -2 V.

The new test waveforms and patterns of the five major factors, resulting from the application of the Taguchi method, are shown in Fig. 17 and described as follows:

(1) Gate voltage high: +17 V; low: -15 V.
(2) Pulse width: 2000 μs.
(3) Data voltage high: +19 V; low: -7 V.
(4) Pulse width: 7000 μs.
(5) Common voltage: -4 V

2. Location Performance Improvement Regarding Line Defects

Four TFT glass substrates, each with a shorted-line defect, were applied as samples to verify the location performance by using the Taguchi method. This entailed increasing the data high voltage to saturate all the pixels on a line, such that the most distant pixel from the point of shortage would still have the greatest noise immunity from the short. However, pixels located near the point of shortage could still be shorted. Thus, the short defect location performance may be increased in this instance. The original test waveforms and patterns of the five major factors are shown in Fig. 17. The new ones, for which the Taguchi method was applied, are shown in Fig. 18, in which the data high voltage is shown to have increased from 19 V to 25 V.

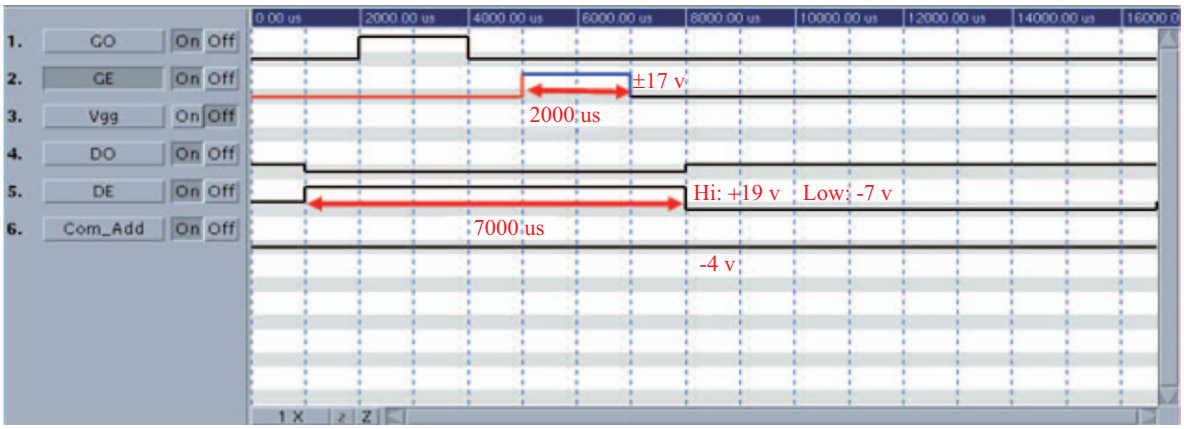


Fig. 17. New test waveforms and patterns.

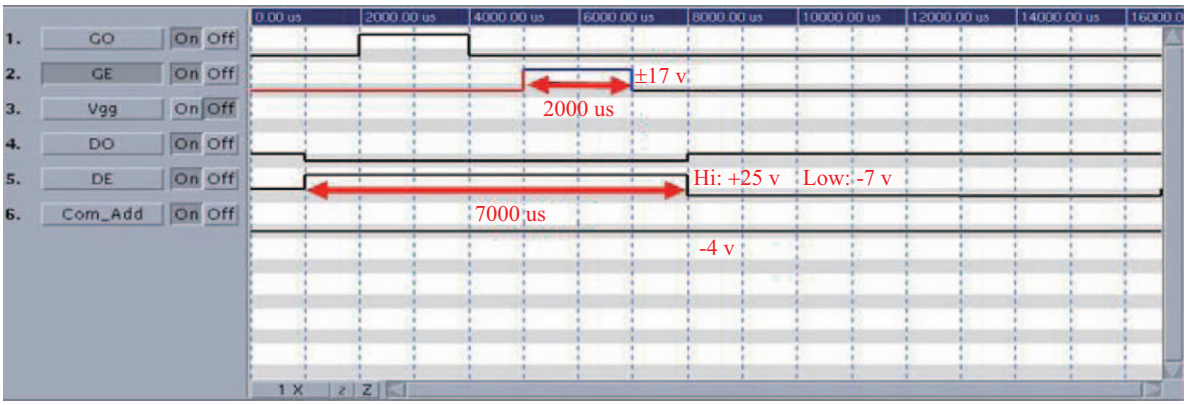


Fig. 18. New data high voltage is 25 V.

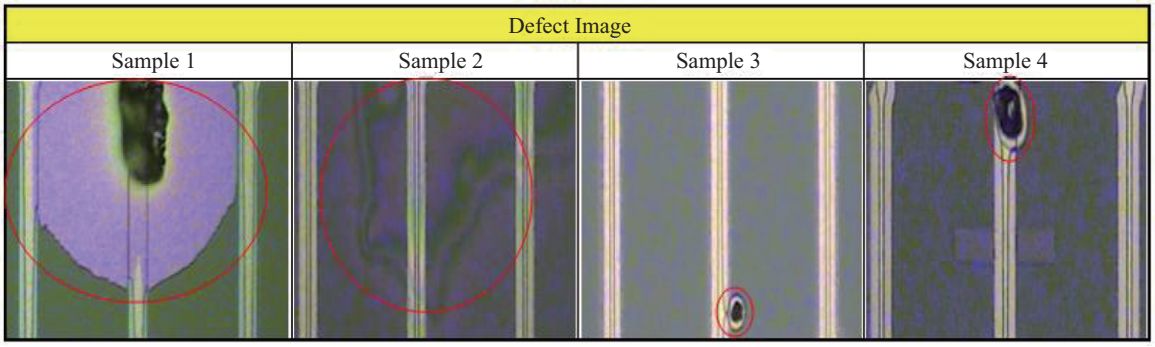


Fig. 19. The results of samples with shorted-line defects can be grouped into four types.

One can group the results of samples with shorted-line defects into four types. Among them, types 1 and 2 exhibited serious shorted-line defects, whereas types 3 and 4 exhibited slight shorted-line defects, as shown in Fig. 19. In type 1, three data lines were shorted to each other by an unclean particle. In type 2, part of the insulating SiNx layer was absent between the gate and data lines, causing the gate, data, and Vcom lines to short to each other. In types 3 and 4, the unclean particles caused the data lines to distort and short with Vcom. Note that one can increase the location capability for shorted-line defects by raising the voltage of data high, which activates functional pixels, indicating the location of a serious defect comprising a large shorted area. Furthermore, it can not only reduce the length of a slight line defect but also indicate the defect location more precisely, as shown in Figs. 20 and 21.

3. Performance Improvement by Adding Point Detection

The traditional criteria are too restrictive to facilitate using

Fig. 20. Test map of a large shorted area.

Fig. 21. The shorted area is reduced to a line or partial line.

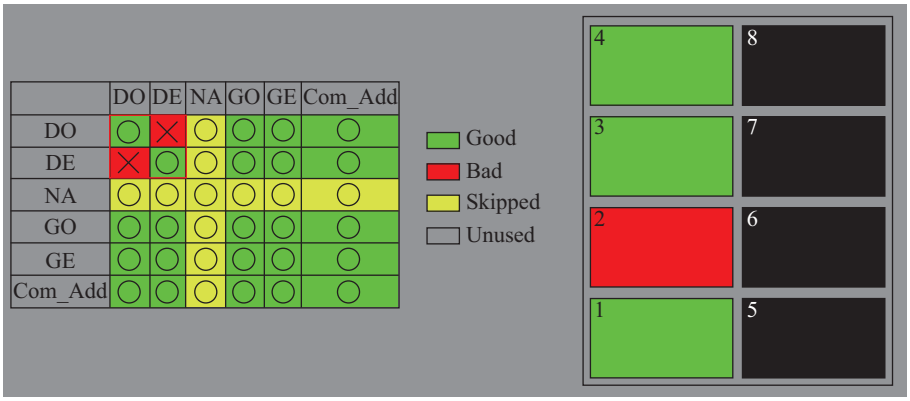


Fig. 22. Improvements from adding point detection.

only one test pattern to detect not only point and line defects but also real false defects. Adhering to these criteria, one cannot find false line defects and increase the location capability simultaneously. According to the experimental results, we propose a method for detecting point and line defects separately. In this method, all the lines on the panel are examined one by one to determine whether they are shorted to each other. As shown on the left side of Fig. 22, two pairs of lines are shorted to each other, as denoted by the red boxes. In this case, the data even line (DE) in the second column is shorted to the data odd line (DO) in the first row, whereas the DO in the first column is shorted to the DE in the second row. As evidenced on the right side of Fig. 22, as a result of point detection, only panel 2 is shorted.

V. CONCLUSION

This paper proposes a novel LCD defect detection method that involves integrating shorting-bar and Taguchi DOE tech-

ologies. The operation principle of the TFT tester entails applying an illuminator to the LCD background panel. If all the TFT arrays are free of failures, then the light from the illuminator can penetrate the scanned pixels (i.e., a bright, complete image should appear on the front display). Otherwise, there are defects in the TFT cells exhibiting dark patterns. Hence, the Taguchi DOE method can be applied to determine the key parameters for the TFT tester design. The simplified test paraeters and conditions can facilitate detecting up to 90% of the faults, whereas the false defect ratio may be increased by as little as 0.34%. Furthermore, the line defect location accuracy can also be increased by adding special runs, thereby improving the test waveforms and patterns. Thus, the proposed method provides a more favorable compromise among the requirements of a higher yield rate, lower production cost, and greater productivity.

REFERENCES

Aoki, H. and T. Nagashima (1998). LCD panel test apparatus. U.S. Patent 5,734,158 A.

Bosacchi, B. (2000). Testing method and apparatus for flat panel displays using infrared imaging. U.S. Patent 6,111,424.

Crawford, G. (2005). Flexible Flat Panel Displays. Publications/John Wiley & Sons, Chichester, England.

Henley, F. J. and S. Barton (1992). Method and apparatus for testing LCD panel array prior to shorting bar removal. U.S. Patent 5,081,687.

Henley, F. J. and S. Barton (2002). Method and apparatus for testing LCD panel array prior to shorting bar removal. U.S. Patent RE 37,847 E.

Hsieh, K. L. and Y. S. Lu (2008). Model construction and parameter effect for TFT-LCD process based on yield analysis by using ANNs and stepwise regression. Expert Systems with Applications 34(1), 717-724.

Jenkins, L. C., R. J. Polastre and R. L. Wisnieff (1992). Functional testing of TFT/LCD arrays. IBM Journal of Research and Development 36(1), 59-68.

Lalama, S. J. (1994). Flat panel display manufacturing overview. 16th IEEE/CPMT International Electronic Manufacturing Technology Symposium 1, 185-190.

Lin, C. F., C. C. Wu, P. H. Yang and T. Y. Kuo (2009). Application of Taguchi Method in Light-Emitting Diode Backlight Design for Wide Color Gamut Displays. Journal of Display Technology 5(8), 323-330.

Liu, C. F., C. T. Pan, Y. C. Chen, Z. H. Liu and C. J. Wu (2013). Design and fabrication of double-sided optical film for OLED lighting. Optics Communications 291, 349-358.

Oshimi, T. and I. Takahashi (1995). Method and apparatus for testing TFT-LCD. U.S. Patent 5,428,300.

Wang, C. C. (2010). Flat panel display manufacturing. U.S. Patent 7,851,141 B2.

Yang, J. F., W. J. Sah and C. L. Ting (2001). Apparatus for testing flat panel display. U.S. Patent 6,281,701 B1.