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UNBALANCED LOAD COMPENSATION IN THREE-PHASE POWER SYSTEM WITH A CURRENT-REGULATED DSTATCOM BASED ON MULTILEVEL CONVERTER

Wei-Neng Chang, Ching-Huan Liao, and Po-Li Wang

Key words: DSTATCOM, FHB converter, load compensation.

ABSTRACT

In this paper, a current-regulated distribution-level static synchronous compensator (DSTATCOM) is proposed for real-time unbalanced load compensation in three-phase electric power distribution systems. The main circuit of the DSTATCOM uses multilevel cascade full H-bridge converter with delta-connected configuration, which is suitable for high-voltage, high-power applications. The compensation algorithm of the DSTATCOM is derived in the phasor domain. Preliminary verification of the DSTATCOM is executed with MatLab/SimuLink program. Finally, a hardware prototype is built for testing. Experimental results confirm the effectiveness of the proposed DSTATCOM for real-time unbalanced load compensation.

I. INTRODUCTION

An unbalanced load in a three-phase, three-wire electric power distribution system absorbs undesired negative-sequence current and reactive power, which cause additional losses in the power distribution system and produce unbalanced voltage drop on the distribution line. The unbalanced voltage drop results in unbalanced voltage on the load bus feeding the unbalanced load and affects other sensitive loads connected at the same bus. Hence, the negative-sequence current and reactive power demands should be improved for keeping good power quality (Heydt, 1991). Unbalanced load compensation, which includes phase balancing and unity power factor correction, is very important for electric power distribution system feeding a large capacity of unbalanced load such as single-phase electrical railway systems and electric arc furnace (EAF) loads.

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Since 1970, static var compensators (SVCs) have been widely employed in power industry as compensators for enhancement of power qualities. Thyristor-controlled reactor with fixed capacitor (TCR-FC) type of SVC with delta connection and individual-phase control ability has been used for real-time unbalanced load compensation (Miller, 1982). Recently, due to rapid development of high power switching elements such as IGBTs and IGCTs, static synchronous compensator (STATCOM), which is one of the FACTS elements, has been recognized as next-generation compensator (Ghosh and Joshi, 2000; Hingorani and Gyugyi, 2000; Ghosh and Ledwich, 2002). Compared to existing SVCs, STATCOM has quicker response time and compact structure. The STATCOM for electric power distribution system applications is also known as distribution-level STATCOM (DSTATCOM).

Many types of multilevel converters/inverters are used for constructing DSTATCOMs such as diode-clamped converter, flying-capacitor based converter, and cascade full H-bridge (FHB) converter (Lai and Peng, 1996; Peng et al., 1996; Lee et al., 2003). Due to modular structure and lower voltage stress, cascade FHB converter is very suitable for DSTATCOM. For this type of DSTATCOM, Y-connected structure is usually seen (Maharjan et al., 2008; Mishra and Karthikeyan, 2009; Lee et al., 2014; Ota et al., 2015). Recently, due to individual-phase operation ability, delta-connected STATCOM has caused attention (Peng and Wang, 2004; Peng et al., 2010; Hagiwara et al., 2012; Du et al., 2013). Both pulse width modulation (PWM) and staircase modulation can be used for the main circuit of the DSTATCOM. For high efficiency op-eration requirement, staircase modulation is usually used (Rodriguez et al., 2002; Gultekin et al., 2012). Like traditional SVC, cascade full H-bridge converter based DSTATCOM with delta connection and individual-phase control ability can be used for real-time unbalanced load compensation.

In the paper, a DSTATCOM with cascade full H-bridge multilevel converter is proposed for real-time load compensation in three-phase power distribution systems. A current-regulated load compensation algorithm is proposed. The

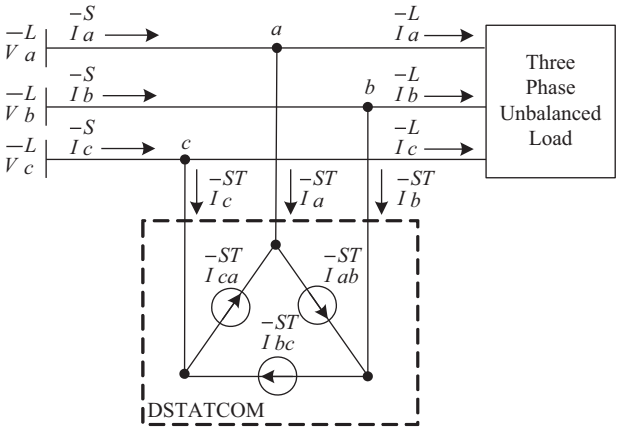


Fig. 1. The studied system with unbalanced load and the DSTATCOM.

DSTATCOM is constructed and simulated with the MatLab/ SimuLink program for preliminary verification. Accordingly, a hardware prototype employing multiple DSP-based systems is built for final verification test. Experimental results show that the proposed DSTATCOM is very suitable for real-time unbalanced load compensation.

II. DSTATCOM COMPENSATION ALGORITHM

Fig. 1 shows the studied system for deriving the compensation algorithm of the current-regulated DSTATCOM. The DSTATCOM is installed in parallel with the unbalanced load for on-site load compensation. The delta-connected configuration of the DSTATCOM main circuit allows individual-phase operation like a traditional static var compensator (SVC) for unbalanced load compensation. In the paper, the DSTATCOM is equivalent as three-phase controlled load currents with unbalanced operation ability.

1. Concept of Load Compensation

In Fig. 1, taking the phase-*a* (to ground) voltage as reference obtains the expression of the three-phase source currents, as shown in (1). In (1), the *R* and *X* in the superscript represent the real and imaginary parts of the source current, respectively. According to the KCL, the summation of three line currents in a three-phase, three-wire system is zero, as shown in (2). Substituting (1) into (2) and separating the real and imaginary parts obtains (3) and (4).

$$\begin{aligned} \bar{I}_a^S &= (I_a^{S,R} + jI_a^{S,X})\angle 0^o \\ \bar{I}_b^S &= (I_b^{S,R} + jI_b^{S,X})\angle -120^o \\ \bar{I}_c^S &= (I_c^{S,R} + jI_c^{S,X})\angle 120^o \end{aligned} \tag{1}$$

$$\bar{I}_a^S + \bar{I}_b^S + \bar{I}_c^S = 0 \tag{2}$$

$$I_a^{S,R} - \frac{1}{2}I_b^{S,R} + \frac{\sqrt{3}}{2}I_b^{S,X} - \frac{1}{2}I_c^{S,R} - \frac{\sqrt{3}}{2}I_c^{S,X} = 0 \tag{3}$$

$$I_a^{S,X} - \frac{\sqrt{3}}{2}I_b^{S,R} - \frac{1}{2}I_b^{S,X} + \frac{\sqrt{3}}{2}I_c^{S,R} - \frac{1}{2}I_c^{S,X} = 0 \tag{4}$$

If the imaginary part of the three-phase source currents are equal, as shown in (5), substituting (5) into (3) and (4) obtains (6). This means that if the imaginary parts of the three-phase source currents are balanced, than the real parts of the three-phase source currents are balanced, too. Furthermore, if the imaginary parts of the three-phase line currents are zero, than the real parts of the three-phase line currents are balanced with unity power factor. This relationship is used to derive the needed compensation algorithm of the DSTATCOM for unbalanced load compensation.

$$I_a^{S,X} = I_b^{S,X} = I_c^{S,X} \tag{5}$$

$$I_a^{S,R} = I_b^{S,R} = I_c^{S,R} \tag{6}$$

2. Derivation of the Load Compensation Algorithm

Equ. (7) expresses the currents of the three DSTATCOM arms (phases) with delta connection in Fig. 1, in which the phase-*a* (to ground) voltage angle is taken as reference. The synthesized DSTATCOM line currents are shown in (8).

$$\begin{aligned} \bar{I}_{ab}^{ST} &= jI_{ab}^{ST}\angle 30^o \\ \bar{I}_{bc}^{ST} &= jI_{bc}^{ST}\angle -90^o \\ \bar{I}_{ca}^{ST} &= jI_{ca}^{ST}\angle 150^o \end{aligned} \tag{7}$$

$$\begin{aligned} \bar{I}_a^{ST} &= \bar{I}_{ab}^{ST} - \bar{I}_{ca}^{ST} = (-\frac{1}{2}I_{ab}^{ST} + \frac{1}{2}I_{ca}^{ST}) + j(\frac{\sqrt{3}}{2}I_{ab}^{ST} + \frac{\sqrt{3}}{2}I_{ca}^{ST}) \\ \bar{I}_b^{ST} &= \bar{I}_{bc}^{ST} - \bar{I}_{ab}^{ST} = (I_{bc}^{ST} + \frac{1}{2}I_{ab}^{ST}) - j\frac{\sqrt{3}}{2}I_{ab}^{ST} \\ \bar{I}_c^{ST} &= \bar{I}_{ca}^{ST} - \bar{I}_{bc}^{ST} = (-\frac{1}{2}I_{ca}^{ST} - I_{bc}^{ST}) - j\frac{\sqrt{3}}{2}I_{ca}^{ST} \end{aligned} \tag{8}$$

Equ. (9) shows the unbalanced load currents in a three-phase, three-wire power system. Use of (10) calculates the three-phase source currents in Fig. 1. Substituting (8) and (9) into (10) obtains (11).

$$\begin{aligned} \bar{I}_a^L &= (I_a^{L,R} + jI_a^{L,X})\angle 0^o \\ \bar{I}_b^L &= (I_b^{L,R} + jI_b^{L,X})\angle -120^o \\ \bar{I}_c^L &= (I_c^{L,R} + jI_c^{L,X})\angle 120^o \end{aligned} \tag{9}$$

$$\begin{aligned}\bar{I}_a^S &= \bar{I}_a^{ST} + \bar{I}_a^L \\ \bar{I}_b^S &= \bar{I}_b^{ST} + \bar{I}_b^L \\ \bar{I}_c^S &= \bar{I}_c^{ST} + \bar{I}_c^L\end{aligned} \tag{10}$$

$$\begin{aligned}\bar{I}_a^S &= (\frac{-1}{2}I_{ab}^{ST} + \frac{1}{2}I_{ca}^{ST} + I_a^{L,R}) + j(\frac{\sqrt{3}}{2}I_{ab}^{ST} + \frac{\sqrt{3}}{2}I_{ca}^{ST} + I_a^{L,X}) \\ \bar{I}_b^S &= (I_{bc}^{ST} + \frac{1}{2}I_{ab}^{ST} - \frac{1}{2}I_b^{L,R} + \frac{\sqrt{3}}{2}I_b^{L,X}) - j(\frac{\sqrt{3}}{2}I_{ab}^{ST} + \frac{\sqrt{3}}{2}I_b^{L,R} + \frac{1}{2}I_b^{L,X}) \\ \bar{I}_c^S &= (\frac{-1}{2}I_{ca}^{ST} - I_{bc}^{ST} - \frac{1}{2}I_c^{L,R} - \frac{\sqrt{3}}{2}I_c^{L,X}) + j(\frac{-\sqrt{3}}{2}I_{ca}^{ST} + \frac{\sqrt{3}}{2}I_c^{L,R} - \frac{1}{2}I_c^{L,X})\end{aligned} \tag{11}$$

In (11), the three-phase source currents are represented with respect to the phase-*a* voltage angle. Using the relationship in (12), the three-phase source currents in (11) can be represented by their own phase-to-ground voltage, respectively. Use of (12) yields the imaginary parts of the three-phase source currents, as shown in (13).

$$\begin{aligned}I_a^{S,R} + jI_a^{S,X} &= \bar{I}_a^S \angle 0^o \\ I_b^{S,R} + jI_b^{S,X} &= \bar{I}_b^S \angle 120^o \\ I_c^{S,R} + jI_c^{S,X} &= \bar{I}_c^S \angle -120^o\end{aligned} \tag{12}$$

$$\begin{aligned}I_a^{S,X} &= \frac{\sqrt{3}}{2}I_{ab}^{ST} + \frac{\sqrt{3}}{2}I_{ca}^{ST} + I_a^{L,X} \\ I_b^{S,X} &= \frac{\sqrt{3}}{2}I_{bc}^{ST} + \frac{\sqrt{3}}{2}I_{ab}^{ST} + I_b^{L,X} \\ I_c^{S,X} &= \frac{\sqrt{3}}{2}I_{ca}^{ST} + \frac{\sqrt{3}}{2}I_{bc}^{ST} + I_c^{L,X}\end{aligned} \tag{13}$$

As mentioned in the previous section, taking $I_a^{S,X} = I_b^{S,X} = I_c^{S,X} = 0$ for (13) obtains the proposed compensation algorithm of the DSTATCOM in terms of imaginary part of the load currents, as shown in (14).

$$\begin{aligned}I_{ab}^{ST*} &= (I_c^{L,X} - I_a^{L,X} - I_b^{L,X})/\sqrt{3} \\ I_{bc}^{ST*} &= (I_a^{L,X} - I_b^{L,X} - I_c^{L,X})/\sqrt{3} \\ I_{ca}^{ST*} &= (I_b^{L,X} - I_c^{L,X} - I_a^{L,X})/\sqrt{3}\end{aligned} \tag{14}$$

With the assistance of the current-regulated DSTATCOM using (14), the three-phase source currents after compensation become (15), which are balanced with unity power factor, i.e., $I_a^{S,R} = I_b^{S,R} = I_c^{S,R}$. Combing the three equations in (15) gets $I_a^{S,R} = I_b^{S,R} = I_c^{S,R} = (I_a^{L,R} + I_b^{L,R} + I_c^{L,R})/3$. The source currents with the DSTATCOM compensation are obtained, as shown in (16).

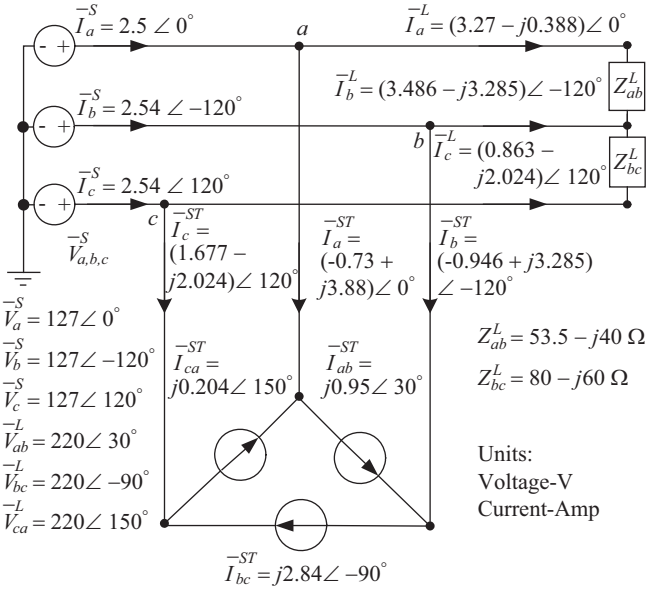


Fig. 2. Illustrating system for the DSTATCOM compensation.

$$\begin{aligned}I_a^{S,R} &= \frac{1}{\sqrt{3}}I_b^{L,X} - \frac{1}{\sqrt{3}}I_c^{L,X} + I_a^{L,R} \\ I_b^{S,R} &= \frac{1}{\sqrt{3}}I_c^{L,X} - \frac{1}{\sqrt{3}}I_a^{L,X} + I_b^{L,R} \\ I_c^{S,R} &= \frac{1}{\sqrt{3}}I_a^{L,X} - \frac{1}{\sqrt{3}}I_b^{L,X} + I_c^{L,R}\end{aligned} \tag{15}$$

$$\begin{bmatrix}\bar{I}_a^S \\ \bar{I}_b^S \\ \bar{I}_c^S\end{bmatrix} = \frac{1}{3}(I_a^{L,R} + I_b^{L,R} + I_c^{L,R}) \begin{bmatrix}\angle 0^o \\ \angle -120^o \\ \angle +120^o\end{bmatrix} \tag{16}$$

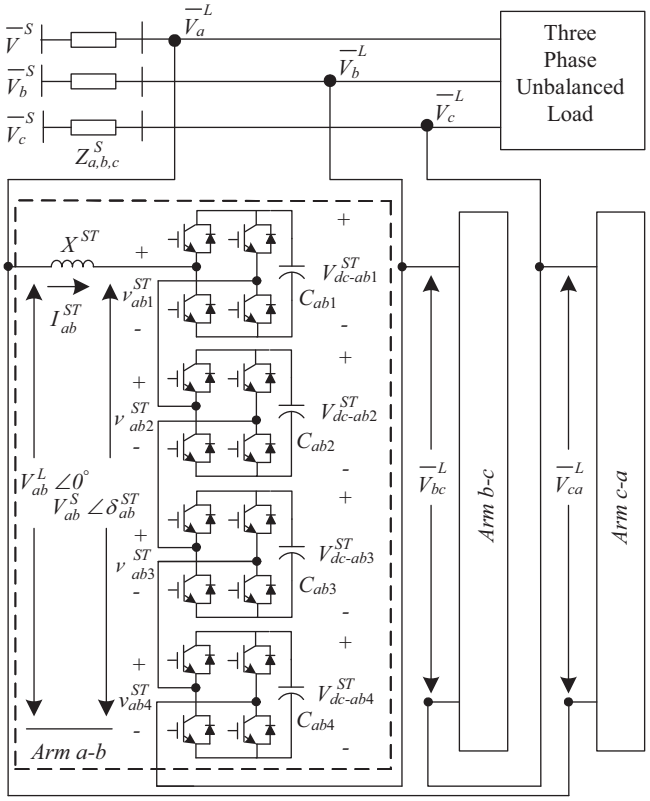
3. Illustrating Example with DSTATCOM Compensation

Fig. 2 presents an example of load compensation with the proposed DSTATCOM. Two single-phase loads are connected in the line *a*-*b* and line *c*-*d*, respectively, which produce unbalanced three-phase load currents. In response, the DSTATCOM generates compensation currents in the three arms by using (14). The three-phase line currents of the load, DSTATCOM, and the power source are calculated in the figure. It is observed that the DSTATCOM offers a way to regulate the power flow between the unbalanced load and the DSTATCOM. As a result, the power source offers balanced three-phase currents with unity power factor, which can also be calculated by using (16).

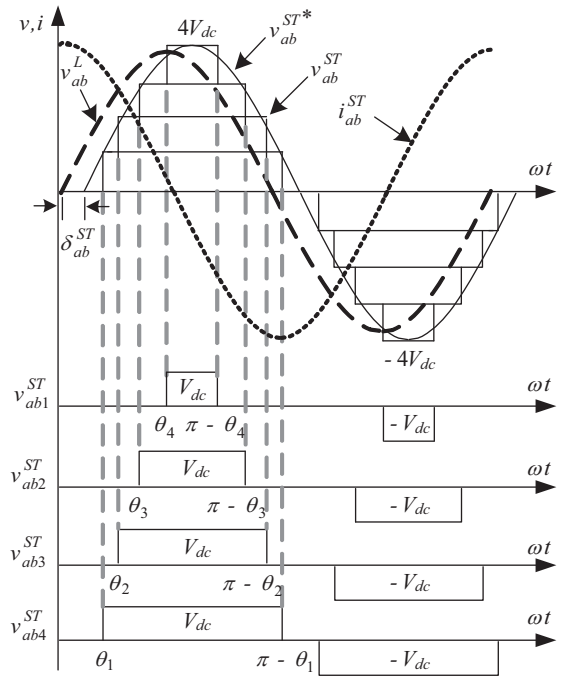
III. DSTATCOM OPERATION PRINCIPLE

1. The DSTATCOM Main Circuit Configuration

Fig. 3(a) presents a three-phase power distribution system with unbalanced load and the main circuit structure of the



(a) Main circuit configuration



(b) Voltage, current waveforms and switching angles of FHB cells

Fig. 3. The DSTATCOM main circuit configuration and waveforms in arm *a-b*.

proposed DSTATCOM. Fig 3(b) shows the voltage, current waveforms and switching angles of FHB cells for the DSTATCOM arm *a-b* in Fig. 3(a). Nine-level cascade FHB converters are used for each DSTATCOM arm, which includes four FHB cells connected in series. Each FHB cell is controlled by switching element such as IGCT or IGBT. DC capacitors are used for the dc links of the FHB cells. Like traditional SVC, the DSTATCOM with delta connection and individual-phase control ability is employed for real-time phase balancing and unity power factor correction. In Fig. 3(a), V_{ab}^{L} is the line-to-line load voltage, V_{ab}^{ST} is the DSTATCOM internal voltage, and δ_{ab}^{ST} is the DSTATCOM internal angle. The power flow of each DSTATCOM arm is expressed in (17) and (18). Each arm current of the DSTATCOM can be operated in inductive, floating, and capacitive modes for the need of load compensation. By regulating the internal angle δ^{ST}, the power source can equally charge or discharge the dc-link voltages of the FHB cells in the DSTATCOM. This changes the DSTATCOM internal voltage V^{ST} and sequentially controls the current flow of the DSTATCOM, as shown in (19).

$$P^{ST} = -\frac{V^{ST}V^{L}}{X^{ST}}\sin\delta^{ST} \tag{17}$$

$$Q^{ST} = -\frac{V^{L}(V^{ST}\cos\delta^{ST} - V^{L})}{X^{ST}} \tag{18}$$

$$I^{ST} = \frac{V^{L}\text{-}V^{ST}\cos\delta^{ST}}{X^{ST}} \tag{19}$$

The voltage waveforms of the DSTATCOM arm *a-b* in Fig. 3(a) is shown in Fig. 3(b). Staircase modulation is employed for each DSTATCOM arm for high efficiency operation. The internal voltage, v_{ab}^{ST}, consists of the outputs of four FHB cells, $v_{ab}^{ST} = v_{ab1}^{ST} + v_{ab2}^{ST} + v_{ab3}^{ST} + v_{ab4}^{ST}$. In Fig. 3, each FHB cell is switched twice in a period of fundamental frequency, which is controlled by switching angles (θ_1, θ_2, θ_3, θ_4). In this way, each FHB cell has three output states, $+V_{dc}$, 0, and $-V_{dc}$. As a result, the DSTATCOM current, i^{ST}, is controlled by the internal voltage v^{ST}. According to (19), the DSTATCOM absorbs capacitive current when the internal voltage is larger than the load bus voltage. On the opposite way, it absorbs inductive current when the internal voltage is smaller than the load bus voltage. The four switching angles, θ_1 to θ_4 should be selected for minimizing the harmonic currents generated.

2. Selection of FHB Switching Angles

The internal voltage waveform v^{ST} in Fig. 3(b) can be represented as a Fourier series, as shown in (20).

$$v^{ST}(\omega t) = \frac{4V_{dc}}{n\pi}\sum_{n=1}^{\infty}[\cos(n\theta_1) + \cos(n\theta_2) + \cos(n\theta_3) + \cos(n\theta_4)]\times\sin(n\omega t) \tag{20}$$

Where: $0 < \theta_1 < \theta_2 < \theta_3 < \theta_4 < \pi/2$

In (20), n is the harmonic order of v^{ST}, where n = 1, 3, 5, 7,…. Ideally, the harmonic orders contain only odd orders without even order harmonic component. The amplitude of each harmonic component in (20) is represented in (21). In (21), taking $n = 1$ yields the fundamental component $H^{ST}(1)$, as shown in (22), which relates the relationship of $H^{ST}(1)$, the dc-link voltage V_{dc}, and the four switching angles (θ_1, θ_2, θ_3, θ_4).

$$H^{ST}(n) = \frac{4V_{dc}}{n\pi}[\cos(n\theta_1) + \cos(n\theta_2) + \cos(n\theta_3) + \cos(n\theta_4)] \quad (21)$$

$$H^{ST}(1) = \frac{4V_{dc}}{\pi}[\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) + \cos(\theta_4)] \quad (22)$$

In Fig. 3(b), the fundamental component $H^{ST}(1)$ is equal to the sum of the dc-link voltages by the control of switching angles, which obtains $H^{ST}(1) = 4V_{dc}$. For a delta-connected DSTATCOM, the triple-order (zero sequence) harmonic currents will circulate in the main circuit of the DSTATCOM. Adequate choice of the switching angles can eliminate the non-triple order harmonic currents. This minimizes the harmonic currents in the synthesized line currents of the DSTATCOM. In order to eliminate the specified harmonic orders, 5th, 7th, and 11th orders, a harmonic minimizing method is employed by setting $H^{ST}(5) = H^{ST}(7) = H^{ST}(11) = 0$ in (21) (Sirisukprasert et al., 2002; Song et al., 2007; Liu et al., 2009). From the aforementioned considerations for the fundamental component and additional harmonic controls, the switching angles are calculated by using (23).

$$\begin{aligned}
&\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) + \cos(\theta_4) = \pi \\
&\cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) + \cos(5\theta_4) = 0 \\
&\cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3) + \cos(7\theta_4) = 0 \\
&\cos(11\theta_1) + \cos(11\theta_2) + \cos(11\theta_3) + \cos(11\theta_4) = 0
\end{aligned} \quad (23)$$

Using Newton-Raphson method for (23) obtains the needed switching angles, $\theta_1 = 10°$, $\theta_2 = 22.2°$, $\theta_3 = 40.8°$, and $\theta_4 = 61.8°$, respectively. With the calculated switching angles, the DSTATCOM can obtain the needed internal voltage and proper harmonic control. During the DSTATCOM operation, the switching signals for the four FHB cells of each DSTATCOM arm are sequentially transported in each period of fundamental frequency. This can balance the dc-link voltages of the four FHB capacitors in each DSTATCOM arm without using dc-link voltage feedback control (Peng et al., 1998; Tolbert et al., 1999; Tolbert et al., 2002).

3. DSTATCOM Controller Design

Fig. 4 shows the proposed DSTATCOM controller in the paper. First, the three-phase instantaneous load currents ($i^L_{a,b,c}$) and load bus voltages ($v^L_{a,b,c}$) are detected to calculate imaginary parts of the three-phase load currents, $I^{L,X}_{a,b,c}$, in real-time. Then, use of (14) calculates the needed compensation currents of the DSTATCOM, $I^{ST*}_{ab,bc,ca}$. The command currents are compared with the actual DSTATCOM arm currents, $I^{ST}_{ab,bc,ca}$. The compared results are send to three PID controllers to generate the internal angle commands, $\delta^{ST*}_{ab,bc,ca}$, for the three DSTATCOM arms, independently. The gains of the PID controller are obtained from a trial-and-error approach. Three phase-lock loops (PLLs) provide three reference angles, $\theta_{ab,bc,ca}$, for the switching patterns generators of the three DSTATCOM arms, respectively. Finally, the internal angle commands are sent to the switching patterns generator to produce gating signals for each DSTATCOM arm's FHB cells.

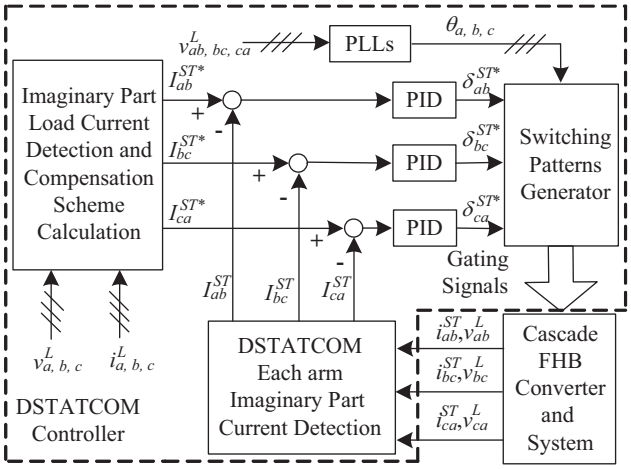


Fig. 4. The proposed DSTATCOM controller.

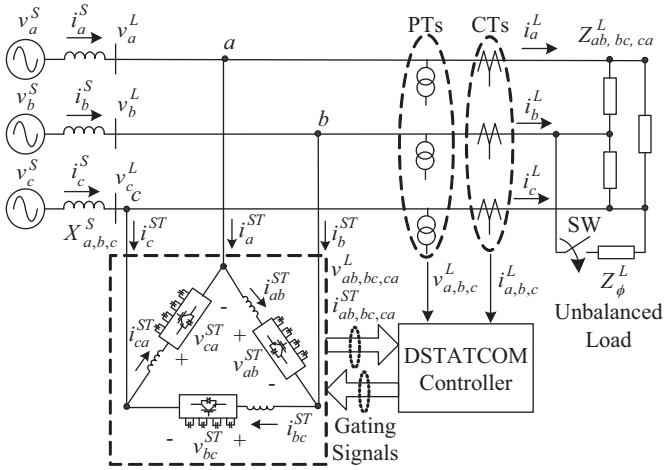
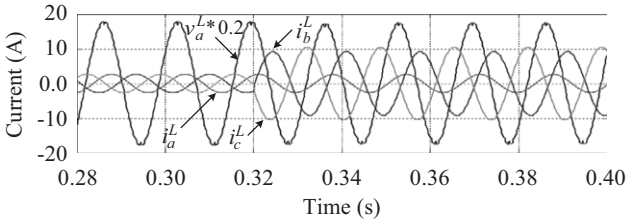


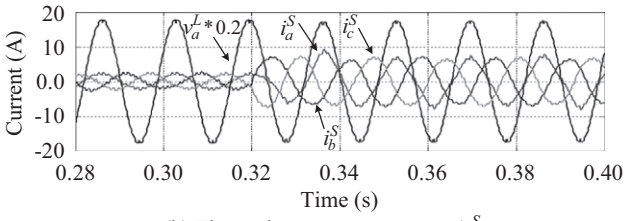
Fig. 5. The DSTATCOM simulation system.

IV. SIMULATION RESULTS

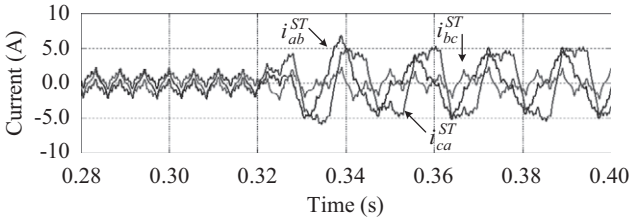
Fig. 5 presents the DSTATCOM simulation system con-



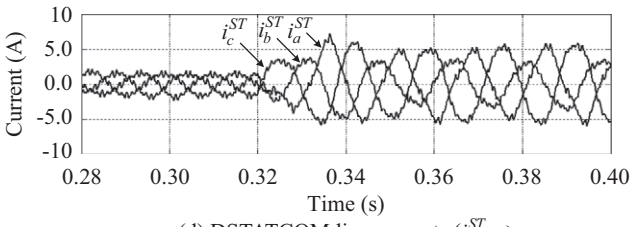
(a) Three-phase load currents ($i^L_{a,\,b,\,c}$)



(b) Three-phase source currents ($i^S_{a,\,b,\,c}$)

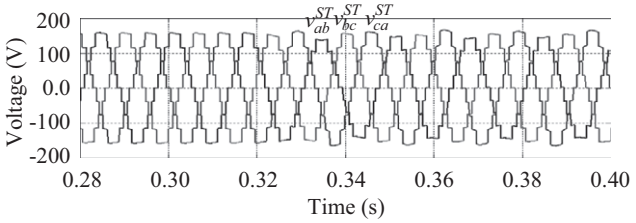


(c) Each arm current of the DSTATCOM ($i^{ST}_{ab,\,bc,\,ca}$)

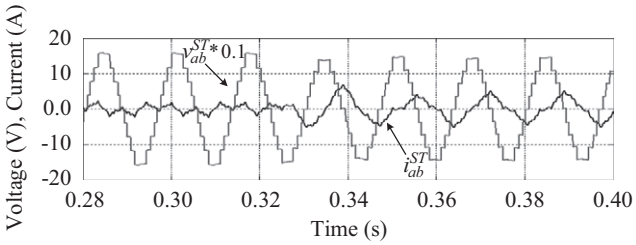


(d) DSTATCOM line currents ($i^{ST}_{a,\,b,\,c}$)

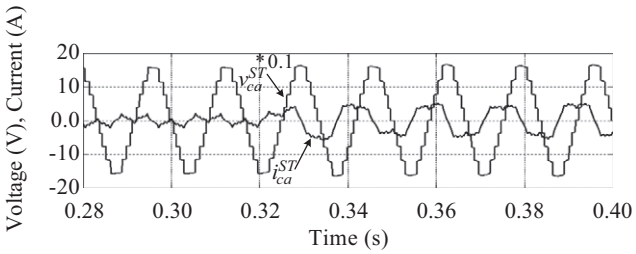
Fig. 6. DSTATCOM compensation result in the simulation.



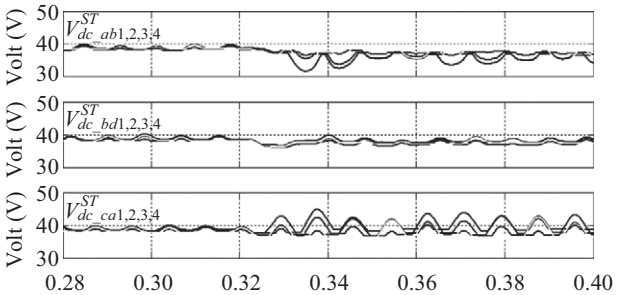
(a) Each arm internal voltage of the DSTATCOM



(b) Arm *a-b* internal voltage(v_{ab}^{ST}) and current (i_{ab}^{ST})



(c) Arm *c-a* internal voltage(v_{ca}^{ST}) and current (i_{ca}^{ST})



(d) Each arm FHB dc-link voltages

Fig. 7. DSTATCOM compensation response in the simulation.

structed in the MatLab/SimuLink program. The DSTATCOM main circuit is a transformerless, delta-connected configuration. An unbalanced load is employed for testing the compensation effects of the proposed DSTATCOM. The Appendix A lists the system parameters in Fig. 5.

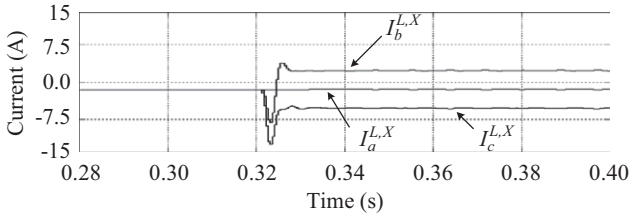
Figs. 6-8 show the simulation results. Fig. 6 presents the DSTATCOM compensation result. At the beginning, the three-phase load currents are balanced with lagging power factor. The switch is then closed to create an unbalanced operation, as shown in Fig. 6(a). With the DSTATCOM compensation, the source currents are compensated to balance and unity power factor, as shown in Fig. 6(b). The compensation speed of the DSTATCOM is quite fast. Fig. 6(c) shows the three arm currents of the DSTATCOM, which contain rich harmonics. By using the harmonics minimizing method in (23), the synthesized line currents contain little harmonics, as shown in Fig. 6(d). Fig. 7(a) is the internal voltage responses of the DSTATCOM, which show that the DSTATCOM changes to unbalanced operation after the load change. Fig. 7(b) shows the transient responses of the current and voltage, i_{ab}^{ST} and v_{ab}^{ST}, in the arm *a-b* of the DSTATCOM. According to the compensation algorithm, the arm *a-b* absorbs inductive current after the change of load. The arm *c-a* absorbs capacitive current at the same time, as shown in Fig. 7(c). Fig. 7(d) illustrates the dc-link voltages responses of the DSTATCOM for reference.

Fig. 8 shows the controller responses of the DSTATCOM in the simulation. Fig. 8(a) presents the calculated imaginary part of the load currents, $I_{a,b,c}^{L,X}$. Fig. 8(b) is the calculated compensation current commands, $I_{ab,bc,ca}^{ST*}$, for each DSTATCOM

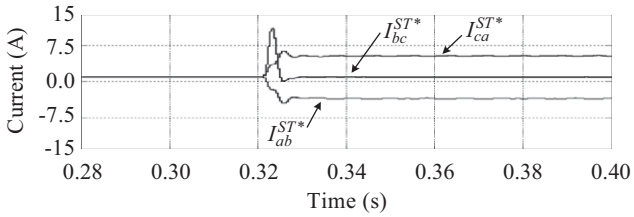
Table 1. Compensation result with the DSTATCOM in the computer simulation.

Load side					
I_a^L	I_b^L	I_c^L	I_1^L	I_2^L	$I_{UR2}^L(\%)$
1.84∠-38°	6.67∠-106°	7.43∠87°	4.87	3.26	66%
Source side					
I_a^S	I_b^S	I_c^S	I_1^S	I_2^S	$I_{UR2}^S(\%)$
4.7∠0.1°	4.7∠-119.7°	4.7∠120.3°	4.7	0.028	0.59%

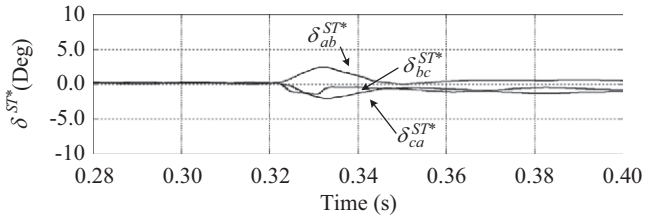
Note: $I_{UR2}(\%) = (I_2 / I_1) \times 100\%$, *unit: Ampere*.



(a) Imaginary-part load currents



(b) DSTATCOM each arm current command



(c) DSTATCOM each arm power angle command

Fig. 8. DSTATCOM controller response in the simulation.

arm. Fig. 8(c) shows the responses of the internal angle commands, δ_{ab}^{ST*}, δ_{bc}^{ST*}, and δ_{ca}^{ST*}. When the three arm currents reach their desired values, the three internal angle commands go back to near zero, independently.

The simulation results in Figs. 6-8 preliminarily confirm the effectiveness of the propose DSTATCOM for real-time unbalanced load compensation. Table 1 lists the steady-state compensation result of the DSTATCOM in the simulation. The unbalance ratio of the load current is 66%. With the DSTATCOM compensation, the unbalance ratio of the source current is improved to 0.59%.

V. HARDWARE TEST RESULTS

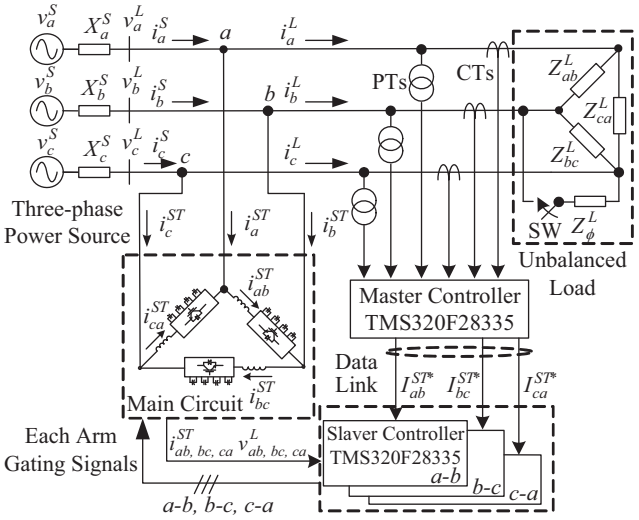


Fig. 9. Structure of the proposed DSTATCOM hardware prototype.

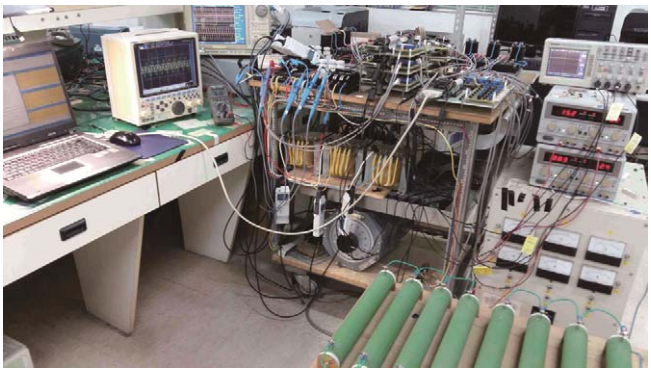


Fig. 10. Photograph of the DSTATCOM hardware setup.

Fig. 9 shows the hardware prototype structure of the DSTATCOM in the paper for final verification. Fig. 10 is the photograph of the DSTATCOM hardware prototype setup. The parameters used in the hardware system are listed in the Appendix B. A balanced, Y-connected inductive load is connected in parallel with a single-phase load for testing. The DSTATCOM main circuit is a transformer less configuration with delta connection. IGBTs are used in the DSTATCOM main circuit as switching elements. Four TMS320F28335 DSP-based controllers are employed to synthesize the controller of the DSTATCOM. One DSP is used as master controller to fetch the load information and calculate the needed compensation current commands of the DSTATCOM. The other DSPs are responsible for each DSTATCOM arm control for generating compensation currents, independently. In practical, this arrangement increases reliability.

Figs. 11 and 12 are the experimental results. Fig. 11 shows the current responses of the test system. At the beginning of the test, the load is balanced with lagging power factor. Then, the switching-in of the single-phase load creates an unbalanced operation, as shown in Fig. 11(a). With the compensation of

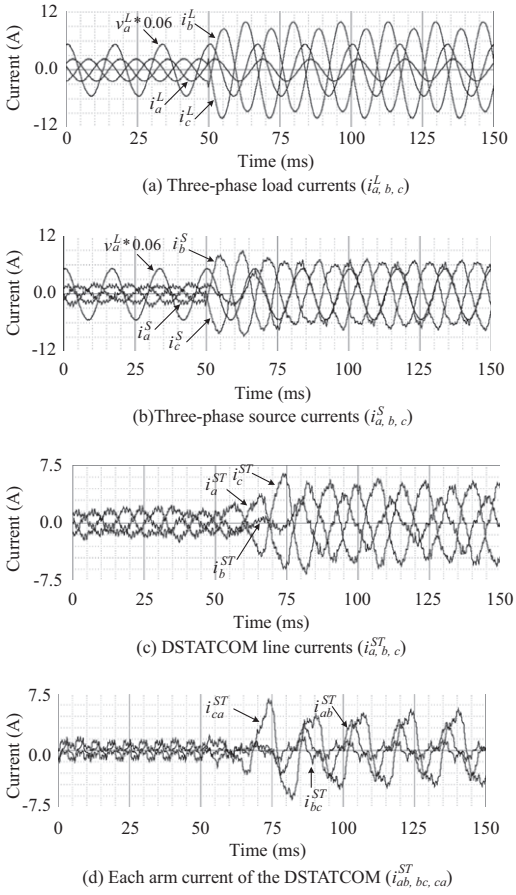


Fig. 11. DSTATCOM compensation response from experiment.

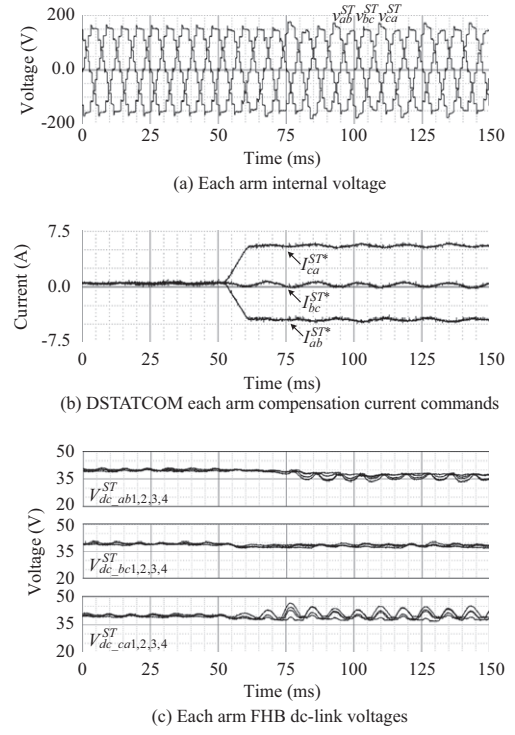


Fig. 12. DSTATCOM controller response in hardware test.

Table 2. Compensation result with the DSTATCOM in the hardware test.

Load	I^L_a	I^L_b	I^L_c	$I^L_{UR}(\%)$
	1.7	6.2	7.2	66.2%
Source	I^S_a	I^S_b	I^S_c	$I^S_{UR}(\%)$
	4.8	5.0	4.7	0.62%

Note: $I_{UR}(\%) = Max\left(\left|I_a - I_{avg}\right|, \left|I_b - I_{avg}\right|, \left|I_c - I_{avg}\right|\right) / I_{avg} \times 100\%$

unit: Ampere.

the DSTATCOM, the source current is corrected very quickly to balance and unity power factor, as shown in Fig. 11(b). Fig 11(c) is the transient response of the synthesized DSTATCOM line currents. Fig. 11(d) is the three arm currents of the DSTATCOM.

A comparison between Fig. 11(d) and Fig. 11(c) shows that use of the harmonics minimizing method and the delta-connected main circuit significantly eliminates the undesired harmonic currents. Fig. 12 shows other responses of the DSTATCOM for reference. Some results in the simulation and the experiment, such as Fig. 8(b) and Fig. 12(b), are slightly different. This difference is mainly caused by time delay of the peripheral circuits, such as D/A converters and isolation amplifiers, implemented in the hardware system. Table 2 lists the steady-state compensation result of the DSTATCOM. The unbalance ratio of the load current is 66.2%. With the DSTATCOM compensation, the unbalance ratio of the source current is improved to 0.62%. Although the compensation algorithm used in the DSTATCOM is very simple, the compensation effect is satisfactory. The experimental results verify that the proposed DSTATCOM is suitable for real-time load balancing and power factor correction.

V. CONCLUSION

In the paper, a current-regulated DSTATCOM with cascade full H-bridge based multilevel converter and delta-connected configuration has been proposed for phase balancing and power factor correction of unbalanced load in three-phase, three-wire power distribution systems. A simple and effective load compensation algorithm derived in phasor domain is introduced for the DSTATCOM. Both the computer simulation and experimental results show that the proposed DSTATCOM is very suitable for real-time unbalanced load compensation. Although the harmonic components in the line currents of the DSTATCOM are not so obvious in the paper, in practical applications, it should be eliminated properly to avoid polluting the power system. Additional functions of the DSTATCOM, such as voltage support, can be implemented with properly tuned auxiliary controllers.

LIST OF SYMBOLS

General:

v: instantaneous voltage

i: instantaneous current
δ: internal angle
V: voltage phasor
I: current phasor
C: dc-link capacitance
θ: switching angle
X: reactance
n: harmonic order
H: amplitude of harmonics

Superscript:

S: source
L: load
R: real part
X: imaginary part
ST: DSTATCOM
ST^*: DSTATCOM compensation command

Subscript:

a, b, c: phase-*a, -b, -c*
ab, bc, ca: line *a-b, b-c, c-a*
dc: dc link
$ab1, ab2, ab3, ab4$: each FHB cell of the arm *a-b*

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APPENDIX

A. Simulation System Parameters

V_{ll}^S = 110 V, f_S = 60 Hz, $X_{a,b,c}^S$ = 0.3 Ω, $R_{a,b,c}^S$ = 0.03 Ω, Z_Y^L = 80 + *j*60 Ω, Z_ϕ^L = 19 Ω, $L_{a,b,c}^{ST}$ = 5 mH, $C_{ab1,2,3,4}$ = $C_{bc1,2,3,4}$ = $C_{ca1,2,3,4}$ = 2,200 μF, $\theta_1 = 10°$, $\theta_2 = 22.2°$, $\theta_3 = 40.8°$, $\theta_4 = 61.8°$, $K_p = 1.22$, $K_I = 0.3764$, $K_D = 0.00087$.

B. Hardware System Parameters

V_{ll}^S = 110*V*, f_S = 60 Hz, Z_Y^L = 80 + *j*60 Ω, Z_ϕ^L = 19 Ω, $C_{ab1,2,3,4}$ = $C_{bc1,2,3,4}$ = $C_{ca1,2,3,4}$ = 2,200 μF, $L_{a,b,c}^{ST}$ = 5 mH, $\theta_1 = 10°$, $\theta_2 = 22.2°$, $\theta_3 = 40.8°$, $\theta_4 = 61.8°$, $K_p = 1.12$, $K_I = 0.3456$, $K_D = 0.0008$.

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